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ANNUAL REPORT

ON

MATERIAL GROWTH AND CHARACTERIZATION DIRECTED TOWARD IMPROVING III-V HETEROJUNCTION SOLAR CELLS

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SUMMARY AND RECOMMENDATIONS FOR FUTURE WORK

The long term aim of this program is the establishment at A & T of a vertically integrated facility capable of fabrication, characterization and testing of optoelectronic devices made of III-V semiconductor compounds.

During the second year (February 1, 1978 to January 31, 1979) of this program, the development of the device processing and testing facilities has moved along satisfactorily. In addition to the existing materials growth laboratory, the photolithographic facility and the device testing facility (Rooms 128 and 130, Cherry Hall) have been completed. The majority of equipment for data acquisition, solar cell testing, materials growth and device characterization have been received and are presently being put to operation.

In the research part of the program GaAs and GaAlAs layers have been grown reproducibly on GaAs substrates. These grown layers have been characterized as to surface morphology, thickness and thickness uniformity (see Tables 1, 2 and 3) using the Nomarski phase contrast microscope, and detailed procedures have been layed out for the preparation and analysis of the layers (see report).

The liquid phase epitaxial growth process has been used to fabricate p-n junctions in $Ga_{1-x}Al_xAs$, where $x \cong 0.1-0.2$. Sequential deposition of two alloy layers (for the development of solar cells has been accomplished. Detailed analysis of the effect of substrate

quality and dopant on the GaAlAs layer quality is presented. Resistivity, mobility, photoluminescence, capacitance-voltage and I-V measurements have been used to investigate the quality of the grown layers and p-n junctions.

Finally, solar cell structures (area $\cong 1.5 \times 10^{-2} cm^2$) were formed by growing a thin p-GaAlAs layer (1-1.5 μm) upon an epitaxial n-GaAlAs layer. The energy gap corresponding to the long wavelength cutoff of the spectral response characteristic was 1.51-1.63 eV. Theoretical calculations of the spectral response were matched to the measured response.

Future work will concentrate on:

1. Improvement in the Hall measurement apparatus.
2. Development of techniques for measuring layers less than a micron thickness.
3. Accurate determination of the diffusion lengths of minority carriers in the GaAlAs alloy layers and the factors which are limiting them.
4. Development of a complete heterostructure device and experimental determination of its efficiency at elevated temperatures and concentrated insolation.
5. Development of processing and testing facility for solar cells and other optoelectronic devices.
6. Growth and characterization of quaternary III-V compounds, with special emphasis on InGaAsP lattice matched to InP.
7. Processing and Testing of Schottky Barrier Field Effect Transistors.

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INTRODUCTION

On February 1, 1977 the National Aeronautics and Space Administration joined Rockwell International Corporation in an effort to develop a solid state electronics program at North Carolina A & T State University. The long term aim of this program is the establishment at A & T of a vertically integrated facility capable of fabrication, characterization and testing of opto-electronic devices made of III-V semiconductor compounds.

The main objective of the development part of the program, specific to the second year, was the establishment of device processing, characterization and testing facilities to complement the already developed materials growth laboratory. The development of a facility for automatic data collection and analysis will be part of the characterization and testing laboratory.

The research part of the program emphasised (a) the growth and characterization of binary (GaAs), ternary (GaAlAs) and quaternary layers on GaAs substrates, and (b) the fabrication and testing of $Ga_{1-x}Al_xAs$ ($0.1<x<0.2$) solar cells that can operate efficiently under high temperature and high intensity conditions.

Laboratory Development

The development of the device processing and testing facilities moved along satisfactorily during this period. Approval was received from the State of North Carolina to continue with the development of

the Solid State Electronics Laboratory. The plans for developing the photolithographic facility and the device testing laboratory were approved and bids were opened May 4, 1978. The construction and renovations of rooms 130 and 132 Cherry Hall started on June 1, 1978. By January 31, 1979, the two rooms were completed specialized equipment were put to operation.

In developing the material and device testing and characterization facility, considerable attention was given to the use of the HP-1000 Computer in connection with automated testing and data acquisition.

The following equipment were ordered and received during this period:

1. Data Acquisition System
   2 HP 59403 A CCI modules
   1 HP 3455 A Digital voltmeter
   1 HP 3495 A Scanner
   1 HP 9872 A Plotter
   1 HP 2645 A Computer terminal with tape drive.
2. Thin film profilometer (Tencor Instruments)
3. Ion beam milling/deposition system (tentative date: May 31,1979)
4. Components of a new LPE/Current Controlled LPE growth facility.
5. X-Y recorders, high current power supplies, semiconductor wafer cutting and polishing facility.
6. Solar simulator

RESEARCH PROGRAM

In accordance with the stated objectives, two liquid phase epitaxy systems were used in the last six months for the growth and characterization of epitaxial layers of GaAs and GaAlAs on GaAs substrates. Details on the experiments undertaken and corresponding results are given below.

GROWTH OF GaAs LAYERS ON GaAs SUBSTRATES BY LPE. DETERMINATION OF SURFACE MORPHOLOGY, GROWTH UNIFORMITY, SYSTEM REPRODUCIBILITY.

The Liquid Phase Epitaxial (LPE) technique has been used extensively to grow GaAs layers of various thicknesses. Two of the most important properties of these layers are their surface and thickness.

Growth of GaAs layers on GaAs substrates took place at 752°C in the system and graphite boat shown in figures 1, 2 and 3. For a single layer deposition, the As saturated Ga melt was slid onto the seed and allowed to equilibrate for 30 minutes as shown in Fig 3b. At this point the ramp generator was turned on and the furnace was allowed to cool down 1°C at a ramp rate of 0.25°C min. The melt was then brought in contact with the substrate as shown in Fig 3c, and after LPE deposition the melt was returned to the neutral position shown in Fig 3a and allowed to cool to room temperature.

Surface Morphology

After termination of the growth cycle, the furnace was allowed to cool to room temperature with the substrate covered. The sample, with a mirror like finish, was removed from the substrate recess. Occasionally a droplet of gallium melt remained on the surface of the epilayer when the melt was wiped from the substrate after termination of the growth. This excess gallium melt was subsequently removed by immersing the sample in warm undiluted HCl for approximately 30 minutes. Then the sample was rinsed thoroughly with DI-H_2O, and blown dry with dry N_2. The sample was then placed in reagent grade methanol and swabbed with a Q-tip to remove any residue left by HCl etch. Using the Zeiss optical microscope with Nomarski interference-

contrast the surface of the epilayer was observed with magnifications of 4x to 40x.

There are many elements that can contribute to obtaining poor surface morphology of GaAs grown layers, such as poor substrate misorientation, and depressions caused by thermal etching and foreign particles on the substrate surface. Without doubt, the most important step in the growth procedure is the substrate preparation.

The photomicrograph of Figure 4 shows the area of the substrate where the melt did not make good contact with the substrate during the growth cycle. As the melt was moved across the substrate, sporadic growth can be observed at the top of the photomicrograph. It is assumed that the sporadic deposition occurred because the substrate was placed in isopropyl over-night which evaporated leaving a thin oxide film on a portion of the substrate. Removal of the film from the surface of the substrate was attempted without success. The horizontal lines at the bottom of the photomicrograph are meniscus lines. These lines correspond to an instantaneous position of the three phase boundary line where the moving liquid gas interface intersects the solid surface. The lines are generated by the stick-slip motion of the melt as it moves across the substrate. The lines are generated by both leading and trailing edges of the melt. Terracing, very typical in LPE growth, was observed on a number of the samples. Figure 5 is a Zeiss interference photomicrograph at 4x, showing terracing. Terraces, unlike meniscus lines, are definite growth steps of variable height which tend to follow lines of constant

epilayer thickness. Saul[3] has studied terraces on "lamellar surface morphology" under a wide range of experimental growth conditions and has shown a dependency on substrate misorientation rather than constitutional cooling. It was also observed that by reducing the vibration of the melt the terracing could also be reduced, but when the larger and heavier boat was used with a number of substrates, vibration did not seem to contribute to terracing.

Another common problem that arises in LPE growth is etch pits. A high density of etch pits was observed on the surface of a number of samples such as the one shown in Figure 6. It was concluded that the majority of the etch pits were generated by thermal etching. Thermal etching exists because GaAs has a significant dissociation pressure of arsenic at typical growth temperatures around 750°C. It was also observed that the thermal etching density is greater on the surface of the substrate than the epilayer, because the substrate is exposed to higher temperatures longer than the epilayer. A graphite cover was constructed for the modified boat to cover the substrate during melt saturation (see figure 2). Thermal etching was reduced considerably by covering the substrate during melt saturation. Workers at Cornell University[4] and also E. Bauser[5] observed that some of the depressions thought to be caused by thermal etching were caused by microscopic foreign particles on the surface of the substrate. These microscopic particles also contribute to cusps. It was observed that the presence of small foreign particles on the substrate surface would only allow epitaxial deposition around the particle as illustrated in Figure 7. Deposition of epitaxial material can only take place where the melt is in contact with the substrate surface. This small

cusp area is usually circular and its diameter is a few micrometers or smaller. In some instances the foreign particles may be completely covered by the epilayer, thus forming cusps or peaks.

Thickness and Uniformity

The thickness is determined by the local growth rate at any point on the substrate which in turn depends on how fast the excess arsenic can be transported from the bulk of the melt to its interface with the substrate. The two primary transport mechanisms for the excess arsenic are by convection and diffusion. It was observed at Cornell University[4] that convection involved circulatory currents in the melt caused by gravimetric instabilities which in turn are caused by certain kinds of temperature and arsenic concentration nonuniformities (i.e., those which tend to make the melt at the top denser than the melt at the bottom). In this study convection is assumed to be negligible because the boat is placed in a constant temperature zone (constant within $0.75^{o}C$) $1/2^{o}C$ to $3/4^{o}C$. The concentration of arsenic (C_{ℓ}) in melt is considered to be constant.

The dependence of epilayer thickness on temperature, cooling rate and time of growth is consistent with theoretical calculations based on the assumption that the growth rate is determined by the rate of solute (As) diffusion toward the interface. That is to say $t \ll \tau$ for the LPE process and since the melt is considered to be semi-infinite and the concentration gradient of the solute (As) in the melt is a constant, then the epilayer thickness (d) can be determined for the ramp cooling case[1] by the use of the theoretical equation

$$d = \frac{4}{3} \frac{R}{C_s} \frac{1}{m} \sqrt{\frac{D_{AS}}{\pi}} \, t^{3/2} \qquad (1)$$

where R is the ramp rate (or cooling rate), C_s is the concentration of arsenic in the solid, m is the slope of the liquidus curve for gallium arsenide, D_{AS} is the coefficient for arsenic and t is the growth time. The above equation indicates that the epilayer thickness (d) is proportional to $t^{3/2}$. There are also theoretical calculations that have led to the conclusion that a large temperature gradient should be established normal to the growth interface in order to prevent constitutional super cooling. However, smooth surfaces were obtained without the presence of a deliberate temperature gradient. In these experiments the melt and substrate were assumed to be at thermal equilibrium.

Thus, the effects of constitutional supercooling can be neglected. Figure 8 is a photomicrograph of a grown layer with the assumption that the temperature gradient that contributes to constitutional supercooling is negligible. The surface was observed to be smooth and uniform.

Dendritic growth of thick layers (7 μm or larger). Sometimes the edge growth is so large that it is impossible to slide the melt from the substrate. Figure 9 gives some indication how the edge growth appears on the substrate. Figure 10 is a cleaved cross section of sample #LR-014-9, showing dendritic growth. One possible explanation for this occurence is that the melt did not cover the surface of the substrate completely during the growth of the epilayer thus causing a substantial edge effect[2] along the line occupied by the meniscus of the melt. This effect consists of a steep sided ridge projecting from the surface of the epilayer and an inhibition of the growth of the epilayer in adjacent regions which were just inside

the melt. Another possible explanation for the occurrence is that at the interface of the solution the well walls were cooler because the graphite acts as a heat sink for the solution. With the solution cooler at the walls of the well, the growth rate at the edges is much faster than the bulk of the solution. In observing the dendritic growth with two samples, it appeared that the height was approximately reduced by one half when the ramp rate was increased from $0.1^{o}C$/min to $0.2^{o}C$/min. This may not be conclusive since only one sample was grown for each of the two ramp rates.

Once the surfaces were examined using Normarski interference-contrast, the samples were cleaved. The cleaved faces were stained by immersing the samples in a CrO_3:$2H_2O$:HF solution for 5 seconds at room temperature to reveal the interface (p-n junction) between the substrate and epilayer. The thickness measurements were taken in bulk of the sample where it was observed to be more uniform.

A summary of the experiments undertaken on the growth of GaAs layers on GaAs substrates and the corresponding results is given in Table 1.

TABLE 1
EXPERIMENTAL CONDITIONS USED TO PRODUCE EPITAXIAL LAYERS OF GaAs BY THE LPE TECHNIQUE

Sample	Epilayer Thickness (μm)	Growth Time (min)	Dopant Doping Density (cm^{-3})	Melt #	ΔT (°C)	Ramp Rate (°C/min)	SUBSTRATE	COMMENTS
LS001-1	---	60	-----	AL-01 Bake 750°C 12 hrs	6.25	0.1	n	Poor surface quality etch. Back for 5 min
LS001-1	2	30	Ge $\approx 10^{18}$	AL-01	3	0.1	n	T_i was raised ≈ 1°C above T_s before sliding melt on substrate partial nucleation occurred on hald of the substrate and there were excessive etch pits.
LS003-1	2.7	30	Ge $\approx 10^{18}$	A1-02 Bake 750°C 12 hrs	3.25	0.1	n 8.2mils	Epilayer shows nonuniform wetting. Did not change growth procedure.
The cooling fans were removed from the furnace mount in order to reduce or eliminate vibration of the melt thereby reducing terracing								
LR004-1	3.65	30	Ge $\approx 10^{18}$	AL-02	4.5	0.1	n 9.6mils	Layer contains etch pits. Terracing was greatly reduced Epilayer seems to be uniform
LR005-1	1.46	30	Ge $\approx 10^{18}$	AL-03 Bake 750°C 11 hrs	2.5	0.1	---	A portion of the epilayer shows a large etch pit density Back etch for 5 minutes.

LR006-1	2.8	30	Ge $\simeq 10^{18}$	AL-03	3.25	0.1	n 9.4 mils	This sample still contained terracing but smooth in general. GaAs diodes were fabricated
LR007-1	--	30	Ge $\simeq 10^{18}$	Al-04 Bake 750°C	3.5	0.1	n 7.6 mils	Melt was covered with graphite plunger and nonuniform wetting was observed.
LR008-1	2.19	30	Ge $\simeq 10^{18}$	Al-04	3		n 9 mils	Melt plunger omitted, epilayer fairly smooth. Etch pit density low.
LR009-1	1.40	30	Ge $\simeq 10^{18}$	AL-04	3.25	0.1	SI	Etch density very low but terracing increased.
LR010-1	3.0	60	Ge $\simeq 10^{18}$	Al-05 Bake 750°C 12 hrs	7	0.116	SI	Terracing increased. There was an attempt to produce a Hall sample
LR011-1	4	45	Ge $\simeq 10^{18}$	Al-05	9	0.19	SI	

A new boat was introduced to the system. The boat was baked out at Cornell University at very low pressures, The boat was also baked out a N.C. A & T S U. using two dummy melts, the growth procedure with this boat is to initiate the growth on the seed for approx 1°C and then slid to substrate.

LR012-1	4.38	30	--	AL-06 Bake 750°C 24 hrs	7	0.2	n	Substrate was polished at Cornell University using bromine methanol. The first run had poor surface quality
LR012-2	2.55-4.38	38	--	AL-06	8	0.2	n	Nonuniformity of epilayer. The layer seems to grow faster on one end than the other
LR012-3	4.05-25.55	60	--	AL-06	11.25	0.2	n	Same as above
LR012-4	2.74	15	--	AL-06	3.5	0.2	n	Very high density of etch pits on a portion of the epilayer
LR012-5	5.55	30	--	AL-06	6	0.2	n	Surface fairly uniform over large area of epilayer
An attempt to elimate the non-uniformity of the epilayer. The shaft for T/C # was sealed to prevent the circulation of outside air, thereby reducing a transverse temperature gradient across the boat.								
LR013-1	5.8	45	--	AL-06 Bake 752°C 17 hrs	8.75	0.2	n	Very uniform surface with the exception of minor terracing
LR013.2	10.95	60	--	AL-07	11	0.2	n	Increase in terraces and etch pits

II. LIQUID PHASE EPITAXIALLY GROWN HOMOJUNCTIONS IN GaAlAs ($Ga_{1-x}Al_xAs$, $0.1<x<0.2$) FOR SOLAR CELL APPLICATIONS

In this part of the research, the liquid phase epitaxial growth process has been used to fabricate p-n junctions in $Ga_{1-x}Al_xAs$, where $x \approx 0.1$-0.2. The resulting structure has applications in solar cells operating at high temperatures and high insolations.

At a solar cell temperature of 300K, an energy gap in the semiconductor corresponding to that of GaAs appears to yield the most efficient cell operation. At elevated temperatures (400-500K), the optimum energy gap shifts to a slightly larger value[7,8] (See Fig.11). Also, several theoretical studies[9,10,11] have shown that a cell structure which incorporates two or more junctions, either in cascade or coupled to specific portions of the spectrum by means of mirrors and filters, can utilize more completely the solar spectrum and operate at higher efficiencies. The energy gap of the top cell, in a two-cell cascade, is about 1.59eV, corresponding to an aluminum mole fraction (in the GaAlAs homojunction cell) of 15%.

It is the high temperature concentrator solar cell and the multijunction solar cell potential for achieving high conversion efficiency that have prompted this research on GaAlAs homojunctions.

Material Preparation and Evaluation Techniques

In order to study $Ga_{1-x}Al_xAs$ homojunctions it is necessary to sequentially deposit two alloy layers by liquid phase epitaxy. The system for performing this is shown schematically in Fig. 12. A diagram of the horizontal boat/slider assembly is shown in Fig. 13.

LPE Growth Procedure

Before a growth sequence is begun, 99.9999% gallium (Alusuiss Metals, Inc., Fort Lee, NJ) is weighed out (2-3 grams) into the melt wells and baked 8-12 hours at 800°C in flowing hydrogen. After cooling to room temperature, cleaned and etched pieces of Si-doped GaAs are added to the Ga melts. The amounts added are slightly less than those required to saturate the melts at the growth temperature. If tin is to be used as a dopant, it is also added at this time. The melts are then baked overnight again at 800°C. This procedure reduces the oxygen contamination and volatile impurity concentration in the melts and graphite boat.

After weighing the Ga into the boat, the weights of the other components of the melt are calculated. The amount of Al is determined from Figure 14. Increasing the amount of Al in a Ga melt reduces the arsenic solubility. The results of computer calculations demonstrating this effect are shown in Figure 15. An approximate melt composition for a 15% AlAs alloy is: 2-3 g Ga, 50-70 mg GaAs and 1 mg Al. The accuracy of weighing such small amounts of aluminum is limited to about $\pm$ 10%.

When the melt purification process is completed, the substrate and source seeds are prepared for growth. This involves the cleaning and etching of vendor polished GaAs wafers, (100) oriented and cleaved to 1.0x1.2 cm to fit the boat depressions. The thickness of these wafers is 0.2-0.225 mm, which provides 25-50 μm of clearance beneath the slider. The substrate and seeds are loaded in a laminar flow hood adjacent to the hood containing the furnace. Dopants, other than Sn, are added to the melts also.

After the vacuum pumping/H_2 backfill sequence, the furnace is raised to the growth temperature. When the furnace has stabilized (one to two hours) the slider is moved from the neutral position to place the melts over the respective source seeds. This is the saturation phase of the growth cycle. When saturating a freshly prepared melt this period should be at least four hours to insure a homogeneous melt composition.

The actual growth phase begins with a supercooling of the melt by 2-3^{o}C. This is achieved by linearly decreasing the furnace temperature at a rate of -0.1 to -0.5^{o}C/min. A standard rate for many of the growths in this study was -0.2^{o}C/min. During this supercooling period the melts are still in contact with the source seeds. Thus, a non-equilibrium solute distribution is established in the melt as regrowth occurs upon the source seeds. At the end of the supercooling period the slider is adjusted to position the melt corresponding to the first eqitaxial layer over the substrate. With the slider in this condition, the second melt is no longer in contact with a source seed. As the furnace termperature continues to decrease the second melt becomes increasingly supersaturated. As long as the temperature decrease is limited to 10-15^{o}C during the growth from the first melt, however, there should be no spontaneous nucleation occurring in the second melt.

The excessive supersaturation of the second melt could be elimated by providing a third source seed in contact with this melt during the first layer growth. An alternative solution is to re-equilibriate the second melt on its source seed after the growth of the first layer. In this condition the furnace temperature could even be raised to insure dissolution of all nucleated material.

However, it was discovered that growth of a second LPE layer upon an epitaxial $Ga_{1-x}Al_xAs$ must be initiated within seconds after removing the first melt from the substrate. If the time during which the LPE $Ga_{1-x}Al_xAs$ is exposed to the hot hydrogen atmosphere is more than a few seconds, the next layer will not uniformly wet the first layer. Non-uniform wetting by the melt results in a very poor quality epitaxial layer.

Substrates

In the growth of the solar cell structures Si-doped GaAs substrates with a carrier concentration of about $2x10^{17}$ cm^{-3} were used (Atomergic Chemetals Corp.). Higher carrier concentrations and Sn doping are desirable, but such substrate materials were not available during the period of this research. Chromium-doped semi-insulating GaAs substrates (also Atomergic Chemetals Corp.) were used for the growth of epilayers to be characterized by van der Pauw resistivity and Hall coefficient measurements. Scrap pieces of the Si-doped material were used as the arsenic source to approximately saturate the melts.

Dopants

The impurity dopant materials which are practical for use in this growth technique are limited in selection. The possibilities among the p-type dopants for GaAs and GaAlAs are: Zn, Ge, Mg, Be, and Mn. Manganese appears as a fairly deep acceptor in GaAs, lying 0.085 eV above the valence band[12]. There is not much information available on the use of Mn as a dopant in LPE growths.

Beryllium is suitable for achieving high carrier concentrations in GaAs and GaAlAs ($>10^{18}cm^{-3}$) [13]. However, it is extremely toxic, oxidizes rapidly, and has a very large distribution coefficient in GaAs (≈ 3). These properties make Be impractical to use as a dopant

in the liquid phase epitaxy system.

Similar to Be in doping properties, magnesium does not suffer the problems of toxicity. In GaAs and GaAlAs, magnesium can be used to achieve carrier concentrations in the upper $10^{18}cm^{-3}$ range[14]. Magnesium has also been observed to improve the wetting of GaAs LPE layers grown on $Ga_{.7}Al_{.3}As$ layers[15]. This effect is apparently the result of the highly reactive nature of Mg. Unfortunately, this reactivity makes it difficult to prevent oxidation of the Mg during melt preparation and exposure to the atmosphere. The distribution coefficient is quite large. A melt doped with 0.5 Mg per gram of Ga results in a p-type GaAs layer with a carrier concentration of about $10^{19}cm^{-3}$.

Some relatively impure Mg ribbon was used to dope a melt containing a high Al concentration ($x^{s}_{AlAs} \cong 0.9$). The resultant growth was characterized by areas of nonwetting and consequently no growth. This is a result of the excessive amount of oxides on the melt surface. Magnesium should be useful as a dopant in the large bandgap window layer to achieve a low sheet resistance.

Another desirable property of magnesium in the fabrication of the cell structure is that it has a relatively large diffusion coefficient in GaAs. The diffusivity of Mg in GaAs at 900°C is reported to be $1.3 \times 10^{-12}cm^2/sec$. An alternative cell structure to be investigated would follow these fabrication steps:

(a) Grow n$Ga_{.85}Al_{.15}As$ active base region

(b) Grow p(Mg) $Ga_{.15}Al_{.85}As$ window layer

(c) Grow p(Mg) GaAs surface contact layer

(d) Diffuse Mg from layer (b) into layer (a) to form active homojunction

(e) Selectively etch the (c) GaAs contact layer away, except under contact grid.

The diffusion process (d) would be performed by raising the LPE furnace temperature after the growths were completed.

Some preliminary Mg doping experiments were performed in GaAs, using Alfa Ventron 99.99% purity Mg chips. GaAs layers were grown upon 2 x $10^{17}cm^{-3}$ Si-doped nGaAs at 800°C with approximately 0.2 at % Mg in the melt. A section of the substrate-epilayer was cleaved off to observe the epilayer thickness with an optical microscope. A photomicrograph of the cross-section at the dendritic edge of the epilayer is shown in Figure 30(a). The epilayer thickness away from this edge is about 6 μm. The remaining portion of the substrate-epilayer was then placed in the LPE furnace and heated at 850°C for five hours. A photomicrograph of a cleaved cross-section of this material is shown in Figure 30 (b). The stained boundary indicates a movement of the p-n junction into the substrate about 1 μm.

These preliminary results with Mg as a diffused acceptor indicate that the procedure outlined in steps (a) - (e) above may be a viable alternative for the device fabrication process. The presence of Mg in the Ga-Al-As melt compounds the oxide problem. Also, because of the relatively high vapor pressure of Mg, the LPE graphite boat design would require attention to restricting the possibility of vapor

phase doping or contamination of the n-GaAlAs melt.

Zinc has been used as a p-type dopant in the GaAlAs-GaAs heterostructure solar cells described by Hovel and Woodall[16]. The distribution coefficient of Zn in GaAs is about 0.4[12]. This makes Zn convenient to use for preparing a melt. The undesirable feature of Zn is its high vapor pressure which causes it to evaporate from the melt at LPE growth temperatures. In one experimental growth, 18 mg of Zn were added to Ga-Al-As melt. After two hours at 750°C, visible deposits could be observed upon the quartz furnace tube and push rod outside the ends of the furnace. It is probable that the Zn vapor would dope the substrate surface and the n-type melt. This high volatility is unfortunate because Zn exhibits a large diffusion coefficient in Gaas (and an even larger diffusion coefficient in GaAlAs[17]). This property is utilized by Hovel and Woodall in their GaAs window layer solar cell[16] to form a p-n junction in the GaAs substrate during LPE growth of a $Ga_{.1}Al_{.9}As$ Zn-doped window layer.

The final acceptor impurity considered in this research is germanium With a distribution coefficient of about 0.01[12], Ge is conveniently weighed in the quantities required for melt preparation. Germanium is an amphoteric dopant in GaAs, however, under LPE growth conditions the Ge atoms preferentially occupy As vacancy sites and behave as electron acceptors. In $Ga_{1-x}Al_xAs$ alloys the acceptor energy level increases linearly with increasing Al composition[18] in the range $0<x<0.55$. Thus, the net carrier density for a fixed Ge concentration

in the solid alloy will also decrease as x_{Al}^{s} increases. Other than the singular growths of GaAlAs and GaAs with Mg and Zn dopants, all the p-type LPE growths were doped with Ge in this research.

The donor impurities which may be used for doping LPE GaAs and $Ga_{1-x}Al_xAs$ are Te and Sn. Selenium and sulfur are volatile elements, and silicon can cause problems because of its amphoteric nature. Tellurium and Sn represent the opposite extremes of distribution coefficients. Sub-milligram quantities of Te are required, which are difficult to weigh. Also, impurities with large distribution coefficients will deplete from the melt more rapidly than those with lower coefficients.

Tin, on the other hand, has a very low distribution coefficient and negligible vapor pressure at 750°C. Because of the low distribution coefficient, large quantities of Sn must be added to the melt which affect the growth morphology and prevent the achievement of planar layer interfaces[19].

In the growth of Sn-doped GaAlAs material by liquid phase epitaxy, the large amount of Sn involved requires that the Al-Ga-As-Sn quaternary system be studied. The effect of adding Sn is to increase the distribution coefficient for the Al component in the liquid and solid phases.

Only tin doping was utilized in this research for n-type layers. with Melt concentrations in the 10-20 atomic % range no surface morphology problems could be associated with the dopant.

Surface Examination

At the completion of a growth the substrate is wiped gently with a cotton swab under warm trichlorethylene to remove the excess Ga droplets. The surface morphology is then examined with a microscope (50-500 X).

A mirror smooth cross-section is obtained by cleaving with a tungsten carbide scriber. The epilayer is stained by dipping the section into room temperature A-B etch.. The etch will quickly dissolve high Al content epilayers. These growths are better decorated by holding the cleaved section in hydrochloric acid fumes for a few seconds, then rinsing with methanol thoroughly. The layer cross-section is then scanned with the microscope to observe the thickness and uniformity.

Resisitivity and Hall Coefficient

In order to characterize the electrical transport properties, layers were grown upon semi-insulating Cr-doped GaAs substrates. These layers should be greater than approximately 5 μm thick to avoid the influence of the surface and interface upon the measured bulk properties.

Sections of the substrate/LPE layer were cleaved to form approximately 4 mm x 4 mm squares. These squares were waxed to a section of a microscope slide with glycol phthalate. Then a stainless steel mask in the shape of van der Pauw cloverleaf pattern[20] was waxed to the LPE layer, also with glycol phthalate. This mask is shown in the drawing in Figure 16. Excess wax was removed by spraying with acetone.

The above assembly was dipped into a room temperature Caro etch for 15 minutes to etch through the epilayer around the mask. After removing the wax, the GaAs samples are etched in hot HCl to remove surface oxides. If the epilayer contains Al, this etch is 25% HCl in methanol for 30 seconds at room temperature.

Ohmic contacts are desired at each of the corners of the mesa pattern. Tin dots are used for the n-type layers. Originally In-3% Zn dots were used for the p-type layers. But, it was discovered that Zn might vaporize and contaminate the mesa surface with a high conductivity layer. Pure In dots were then tried with satisfactory results when the carrier concentration is greater than $1x10^{17} cm^3$.
These metal dots are alloyed on a graphite strip heater in H_2 for two minutes at 450°C. The In contacts are rather fragile, but are pressed into the surface with the spring fingers of the sample holder.

For the resistivity and Hall coefficient measurements the sample in its holder is mounted between the poles of a Varian electromagnet. The sample current is adjusted to yield detectable voltages without introducing significant Joule heating. The voltages are monitored with a Data Precision digital multimeter (0.1mV accuracy). The Hall coefficient is determined at a magnetic flux density of 3 kilogauss. Measurements are performed at room temperature and at 77 K by placing the sample holder in a container of liquid nitrogen.

In the calculations of resisistivity, ρ, and Hall coefficient, R_H, the layer thickness is assumed to be that obtained in the microscopic examination. The carrier concentration relationship is assumed to be $n,p=(qR_H)^{-1}$.

Photoluminescense Measurements

In the direct bandgap regime of $Ga_{1-x}Al_xAs$ alloys ($0<x<0.37$), the energy gap can be approximately determined from the peak energy of the photoluminescence (PL) spectrum at room temperature. This measurement assumes that the most prominent peak is caused by a band-to-band recombination event. Since the absorption coefficient for these alloys is in the 10^4-10^5 cm^{-1} range, only a very thin surface layer is examined by this technique..

Photoluminescense measurements were performed upon a few samples at Research Triangle Institute, Research Triangle Park, N.C. The system consisted of a Spectra-Physics 86 mW He-Ne laser illuminating the room temperature sample through a chopper wheel. The PL radiation was analyzed by a Jerrel-Ash 0.5 meter monochromator with a resolution of about 32 Å. The output of this monochromator was detected by a RCA 7102 photomultiplier tube and amplifier by a PAR 128A lock-in amplifier.

The peak wavelength of the PL signal was noted and related to the alloy Al composition by the equation[21,22].

$$E_g(x) = E_{g1} + bx + cx^2. \qquad (2)$$

where E_{g1} is the direct energy gap of the lower bandgap binary and $E_{g2} = E_{g1} + B = C$; E_{g2} is the direct energy gap of the higher bandgap binary. Experimentally, photoluminescence measurements on a few samples of intermediate composition will enable determination of the constants b and c in Equation (2) for a specific ternary system. The strength and bandwidth of the PL spectrum is somewhat qualitatively related to the degree of perfection of the surface region of the sample. Broad peaks and low amplitude signals appear to result from a high defect density in the material.

Diodes and I-V Measurements

Diodes were fabricated from LPE grown p-n junction structures by metallizing the ohmic contact areas, annealing the contact metals, and cleaving or etching to form the device. The yield rate for satisfactory devices seemed low; this is a result of the presence of defects in the LPE layers and difficulties in processing the very thin surface layer junction.

Contact to the n-type GaAs substrate was made by electron-beam evaporating 750 A^o of Au-12 wt% Ge and 400 A^o of Ni. Prior to evaporation the wafer is cleaned in solvents, and etched briefly in a 1:3 HCL: methanol solution.

Some difficulty was encountered in making a satisfactory ohmic contact to the p-layer. This was partially because the carrier density

was somewhat lower than desirable for achieving a good contact characteristic. Another problem is that of oxide (or possibly a hydroxide) formation on the surface of the GaAlAs. Evaporated Au-Zn can form a suitable contact to p-GaAs or p-GaAlAs after annealing to diffuse the Zn into the surface slightly. However, facilities were not available for evaporating a Zn alloy. An alternative choice was an electron beam evaporated Ag-4 wt% Mn alloy. About 1000 A^0 of this material was evaporated onto the substrate which was heated to approximately 200°C. This surface layer contact was evaporated onto the entire wafer through a metal mask with an array of 0.25 mm diameter holes.

Both the n- and p- contacts were annealed simultaneously on a graphite strip heater in flowing hydrogen for two minutes at 450°C. The Au-Ge eutectic composition generally gave good results on the n-substrates. The Ag-Mn contact to the p-epilayer was not always ohmic.

The best diode characteristics were achieved with diodes formed by cleaving approximately 1 mm square chips after metallization and annealing. In this form the junction is very vulnerable to the formation of shunting paths due to tweezer damage or the metallization forming a short circuit. Etched mesa diodes masked by wax dots were not as successful as the cleaved diodes in yielding good current-voltage characteristics.

Some of the cleaved diodes were cemented to TO-3 transistor headers with a silver conductive epoxy. A 30 μm gold wire was epoxied to the top surface. Neither the epoxy nor the Ag-Mn metallization could withstand any of the mild etches to remove the damage at the junction caused by the cleaving of the chip. This epoxy also failed when the header-mounted diode was dipped in liquid nitrogen. At elevated

temperatures ($\sim$100^{o}C) the epoxy mounted units appeared to become noisy.

Initially, the diodes and contacts were examined with a Tektronix Transistor Curve Tracer. The reverse breakdown voltage was observed during this measurement.

The current-voltage characteristic of the fabricated diodes was measured by varying the bias current and recording the voltage drop. A DC power supply and cascaded potentiometer supplied the current which was monitored by a Keithley Model 174 digital multimeter. A Data Precision DMM was used to measure the diode voltage drop. Light was excluded from the diode during the measurements.

Some n-n isotype heterojunction structures were fabricated from single layer growths of n-GaAlAs on n-GaAs. Both surfaces were metallized with Au-Ge/Ni and annealed.

Capacitance-Voltage Measurements

A Materials Development Corporation Automatic Doping Profiler was used to obtain capacitance versus reverse bias voltage data for some of the diode structures. The measurement frequency was 1MHz. Generally, $1/C^2$ versus V is examined for a linear relationship, indicating an abrupt junction. If the extrapolated contact potential ($1/C^2 \rightarrow 0$) is larger than about one volt, this is an indication of an interface dipole layer or a net interface charge.

Solar Cell Structures

If a LPE grown p$Ga_{1-x}Al_xAs$-n$Ga_{1-y}Al_yAs$ ($x,y \simeq 0.15$) diode exhibited photoresponse to focussed illumination, a test solar cell structure was fabricated from the remaining substrate material. After cleaning the sample surface, a small (1.3x1.3 mm) contact grid pattern was

deposited by evaporating Ag-Mn through a metal mask. The base contact again was evaporated Au-Ge/Ni. These contacts were annealed at 450°C for two minutes. The grid contact outline is shown in Figure 17, and a photomicrograph of a region of an evaporated Ag-Mn contact on a GaAlAs epilayer is shown in Figure 18.

Small rectangles of 100 μm thick mylar were waxed over the individual grid patterns to serve as a mask for the mesa insolation etch. A room temperature 5:1:1 Caro etch was used.

The electrical characteristics of the cell structures were checked with the transistor curve tracer. The yield of satisfactory devices at this point was quite low, presumably a result of the contact metallization short circuiting the active region through pinholes in the epilayers. External electrical connection was achieved with a beryllium copper probe front contact and the sample resting upon a metal plate.

Photoresponse of the Solar Cell Structures

The I-V characteristics of the cells were measured with the transistor curve tracer while illuminating with a 600 watt tungsten halogen lamp. The position of this lamp was adjusted to produce a short circuit current density of 25 mA/cm^2 from a silicon solar cell (antireflection coated) adjacent to the test GaAlAs homojunction cell. This room temperature measurement approximates an Air Mass One insolation.

Spectral response measurements were performed with the system shown in Figure 19. A 100 watt tungsten halogen lamp is focused upon the entrance slit of a Jarrell-Ash 0.25 meter grating monochromator. The output beam diverges and a position was chosen to fully illuminate the reference detector. This was a United Detector Technology, Inc. silicon photovoltaic detector with an active area of 0.2 cm^2. Cali-

bration data (amperes/watt) was provided at 0.025 μm intervals from 0.35 μm to 1.1 μm by the manufacturer.

A low pressure mercury lamp was used to determine the resolution of the monochromator (full width at half maximum intensity). With 1 mm slit widths this value was about 4×10^{-3} μm at 0.546 μm wavelength. This agrees with the 3.5 mμ/mm linear dispersion value stated for the grating.

With the tungsten lamp source the detector was used to measure the monochromator output in the 0.4-0.88 μm range. Then the GaAlAs solar cell was placed in the same position, and its output current was measured. A Keithley Model 174 digital multimeter was used for both these measurements. The test device currents were on the order of tens of nano-amperes. A Corning 3-72 glass filter was used to eliminate second order interference at wavelengths greater than 0.45μm.

SUMMARY OF RESULTS

Liquid Phase Epitaxial Layers

About 50 LPE growth experiments were performed involving single and double layers of GaAs and GaAlAs. Some of the experiments were not successful because of problems encountered with the substrate sliding out of position.

An example of a single GaAlAs growth (sample 14MR78, Table 2) is shown in Figure 20. In the upper photomicrograph in this figure, the surface terracing can be seen to vary between broadly spaced undulations and a much finer pattern near the top of the photomicrograph. In the bottom center of this region can be seen a typical pinhole type of growth defect.

The lower photograph in Figure 20 shows a cleaved, stained cross section of the grown layer. The thickness is about 7.3 μm. This growth was performed upon a Cr-doped GaAs substrate for later resistivity and Hall coefficient measurements. The melt was doped with Ge.

Two successive LPE layers of GaAlAs are shown in the photograph in Figure 21. The surface layer which is Ge-doped, is 1.5 μm thick. The first layer grown from a Sn-doped melt is 6.5 μm thick. A portion of this growth was fabricated into a solar cell structure.

Most of the GaAlAs epitaxial growths were performed from melt compositions calculated to yield 10-20% Al in the solid alloy. A few melts with sufficient Al to yield 90-95% AlAs in the solid were prepared. The growths from these melts were generally of such poor quality that no electrical or optical measurements could be performed upon them.

Photoluminescence Measurements on Epilayers

Photoluminescence (PL) measurements were performed upon several GaAlAs epilayers at room temperature. The results are summarized in Table 2. All the layers appeared visually to be of good quality. The latter four samples reported in Table 2 are those upon which resistivity and Hall coefficient measurements were performed. The wavelength of the peak photoluminescence intensity was noted and converted to the equivalent energy, E_{peak}. By assuming that E_{peak} corresponded to the approximate energy gap of the alloy layer, the Al fraction, x_{Al}, in $Ga_{1-x}Al_xAs$ was calculated with Equation (2). Also measured from the recorded traces were the full spectral width at half maximum intensity (FWHM).

For purposes of a reference measurement, a Si-doped GaAs substrate ($n \simeq 2 \times 10^{17}$ cm^{-3}) was examined. The surface was polished as received from the vendor. The photoluminescence measurement results are indicated in the first line of Table 1. The PL peak was quite broad, as indicated by the FWHM value of 480 A^o. The peak wavelength corresponds approximately to the bandgap energy of GaAs.

Sample 20MR78 did not exhibit any recognizable peak in the PL spectrum. This is indicative of a high defect density in the region of the surface with nonradiative processes dominating the recombination.

The fairly broad PL peak from sample 14SP77 centered at approximately the bandgap energy GaAs is puzzling. The growth of this sample was performed by adding Al to a melt which had previously been saturated with GaAs at 750 ^oC. The growth occurred at 800^oC. Perhaps the Al remained undissolved in the form of AlAs, and therefore the epilayer was virtually pure GaAs.

Table 2. Photoluminescence measurements on epitaxial GaAlAs at room temperature.

Sample	Material	Dopant	Thickness	Results λ_{peak}(a)	FWHM(b)	E_p(c)	x_{Al}
			(μm)	(A^o)	(A^o)	(eV)	
Substrate	GaAs	Si	-	8660	480	1.43	0
20MR78	GaAlAs	Sn	9.0	Noisy spectrum, no peak		-	-
14SP77	GaAlAs	Ge	1.0	8726	500	1.42	0
27MR78	GaAlAs	Sn	3.6	7326	200	1.69	0.25
20DE77	GaAlAs	None	5.0	7421	125	1.64	0.2
20MR78	GaAlAs	Sn	9.0	7632	200	1.62	0.18
14MR78	GaAlAs	Ge	7.3	7985	260	1.55	0.11
7AP78	GaAlAs	Ge	5.5	7539	260	1.64	0.2

(a) λ_{peak} is the wavelength of the peak of the photoluminescence spectrum.

(b) FWHM is the width of the spectrum between the half-intensity wavelengths.

(c) E_p is the energy corresponding to λ_{peak}.

The remaining five samples in Table 1 indicate Al compositions of 0.11 to 0.25, which are in reasonable agreement with the initial melt composition and the liquidus-solidus data. Sample 20DE77 was undoped and exhibited a relatively narrow spectral width of 125 A^o. Dopants (Sn and Ge) added to the melts produced layers with somewhat wider PL peaks. This is probably a result of the merging of the band-to-band and band-to-impurity photoluminescence peaks. Measurements at low temperatures would be desirable to resolve the separate PL spectra of the two recombination paths. At a wave length of 0.75 μm a 200 A^o full width at half maximum intensity corresponds to 0.044 eV.

Figure 22 is a tracing of the photoluminescence spectral emmission of Ge-doped sample 14MR78. This is a typical spectrum for the GaAlAs layers examined.

Resistivity and Hall Coefficient Measurements

From data taken at room temperature (298 K) and liquid nitrogen temperature (77 K), the resisitivity, Hall coefficient, carrier concentration, and Hall mobility of a selection of LPE growth samples were calculated. The results, which compare GaAs samples with low Al concentration alloys, are presented in Table 3. An indication of the purity achievable with this epitaxial system is illustrated by the parameters for undoped GaAs sample (120C77). The analogous GaAlAs alloy sample (20DE77) exhibits carrier concentrations (assuming n,p = $1/R_Hq$) which are about 40 times larger. The origin of the unintentional impurities can only be conjectured, and the large differences in concentrations between the two samples is unexplained. In both cases Si-doped GaAs was used as saturation and source seed material. The melts were supercooled about 2^oC before sliding onto the substrates,

Table 3. Summary of resistivity and Hall coefficient measurements on LPE GaAlAs and GaAs growths.

Sample	Material	Thickness (μm)	Temp. (K)	ρ (ohm-cm)	R_H (cm^3/coul)	μ_H (cm^2/V-sec)	n,p (cm^{-3})	
120C77	GaAs (undoped)	8.0	300	1.8	1.1×10^4	6.1×10^3	5.6×10^{14}	n
			77	0.98	1.3×10^4	1.4×10^4	4.7×10^{14}	
7SP77	GaAs (Ge-doped)	5.11	300	0.12	14.24	121	4.4×10^{17}	p
			77	0.23	141	602	4.4×10^{16}	
2NO77	GaAs (Sn-doped)	7.4	300	.007	31.3	4.5×10^3	2.0×10^{17}	n
			77	.008	34.4	4.5×10^3	1.8×10^{17}	
20DE77	GaAlAs (undoped)	5.0	300	.08	267	3.3×10^3	2.3×10^{16}	n
			77	.07	360	5.3×10^3	1.7×10^{16}	
14MR78	GaAlAs (Ge-doped)	7.3	300	0.13	20.2	152	3.1×10^{17}	p
			77	3.0	931	313	6.7×10^{15}	
7AP78	GaAlAs (Ge-doped)	5.5	300	0.05	5.87	112	1.1×10^{18}	p
			77	2.81	.354	126	1.8×10^{16}	
20MR78	GaAlAs (Sn-doped)	9.0	300	0.013	30.6	2.3×10^3	2.0×10^{17}	n
			77	0.013	32.1	2.4×10^3	1.9×10^{17}	

so there should have been no dissolution of the Cr-doped GaAs substrate to dope the ensuing LPE layer growth.

By comparing the measured Hall mobility and carrier concentration at 77 K of GaAs sample 120C77 with the data of Wolfe and Stillman[25] for the GaAs, a total impurity concentration of $(N_D + N_A) \simeq 1.6 \times 10^{16}$ cm^{-3} is obtained. This is indicative of a large amount of impurity compensation.

To aid in presenting the data in Table 3, the carrier concentrations are plotted as function of 1/T in Figure 23. Although a greater collection of n,p versus 1/T data would be necessary for an extensive analysis of the carrier density temperature dependence, the lines joining the data points for the two temperatures do illustrate overall characteristic behavior.

In Figure 23 the Sn-doped GaAs (2N077) and GaAlAs (20MR78) samples indicate an almost constant carrier concentration over the temperature range. Similar results have been obtained by Panish[19]. The explanation for this is that because of the formation of an impurity band overlapping the conduction band by the very shallow tin donor, a metallic impurity conduction mechanism is exhibited. Thus, the effective donor ionization energy has gone to zero.

The behavior of the carrier concentration in the Ge-doped GaAlAs samples (14MR78 and 7AP78) is similar to the results reported by Springthorpe, et al.[18] for a 21% Al alloy. They found that, as the Al fraction increased in the alloy, the ionization energy for the Ge acceptors increased. This activation energy is obtained by using a curve fitting approach on the p versus 1/T data. With the lack of

adequate data in the present research, the activation energies are calculated from the slope of the straight line joining the 298 K and 77 K data points in Figure 23. For sample 7AP78 this activation energy is $E_A \simeq 0.073$ eV. With a greater detail in the p versus 1/T data for a 20% Al alloy, Springthorpe, et al[18]. obtained $E_A \simeq 0.045$ eV by the same computational technique.

The room temperature carrier concentration data is useful also because it provides the necessary information for preparing the melts to obtain the required solidus impurity concentration.

Current-Voltage Measurements on $Ga_{1-x}Al_xAs$ Homojunctions and nGaAs-n$Ga_{1-x}Al_xAs$ Isotype Heterjunctions

The nGaAs-nGaAlAs isotype heterojunction resulted from the growth of Sn-doped $Ga_{1-x}Al_xAs$ upon Si-doped GaAs substrates (Sn $\simeq 2\text{-}4\times10^{17}$ cm^{-3}, $x \simeq 0.2$). The GaAlAs surface was contacted with Au-Ge/Ni in the form of a continuous layer (for cleaved diodes) and 0.25 mm diameter dots. The current-voltage (I-V) characteristics of the cleaved diodes were generally linear, and any departures from linearity were also observed between dot contacts on the GaAlAs surface. It was assumed therefore, that the non-linearities were a result of poor contacts to the GaAlAs, rather than the internal heterojunction.

In Figure 24 the I-V characteristics of two p-n GaAlAs homojunctions are shown. This data was taken at room temperature. Device D20AP78 is a chip (area $\simeq 4\times10^{-3}$ cm^2) from the substrate used to fabricate a solar cell test device. The measurements were made with a beryllium copper probe contact. Over the current range from 3 μA to 300 μA, this diode has an A_1 factor of 1.91. At the higher currents, the current increases more slowly with voltage. Without more extensive

selection of data, it is impossible to assign a particular mechanism to this high current behavior. The most probable cause is the surface series contact resistance.

Device D6AP78 is a chip (area $\simeq 8 \times 10^{-3}$ cm^2) which was epoxied to a TO-3 transistor header, and contacted with a gold wire and conductive eposy. Over a narrow current range (100 μA to 10 mA), the A_1 factor is about 2.0. At lower currents, the I-V data suggest an excess current due to a linear shunting resistance. This is a frequent result with the diode fabrication techniques employed. Ragged junction surfaces due to cleaving, contamination as a result of tweezer handling and undercutting of the surface metalization during etching will induce surface current paths.

In Figure 25 the I-V characteristics of device D6AP78 room temperature ($25^{o}C$) and $117^{o}C$ are shown. At $117^{o}C$ the A_1 factor is still about 2.0. At this temperature the I-V data eventually became unstable, possibly as a result of contamination from the outgassing epoxy.

Because of the failures of the fabricated diodes due to the development of shunt leakage paths, more extensive temperature data for the devices were not obtained. This data underforward and reverse bias conditions may have aided in determining the controlling current-voltage mechanisms for these LPE grown homojunctions.

Figure 26 is a photograph of the I-V characteristic of D6AP78 at room temperature. Other devices fabricated from this growth or similar material also exhibited reverse breakdown voltages of 8-10 volts.

The p-n junction behavior for these devices can be complicated by the growth technique employed which may create a heterojunction rather than the desired homojunction in GaAlAs. This can occur because

the two melts are not prepared identically, and because the use of Sn as a dopant increases the segregation coefficient for Al. A better quality junction could be formed by diffusion, probably from a Zn source. But this leads to other difficulties in the growth process. A grown junction has the advantage of control of impurity concentration in both active regions.

Capacitance-Voltage Measurements

In Figure 27 the $1/C^2$ versus V_R data for two chip-type GaAlAs homojunction diodes are presented. The C20AP78 data were measured on a chip cleaved from the 20AP78 solar cell LPE growth. The C6AP78 chip was from a double epilayer growth with a surface thickness of 3.5 μm and a n-layer thickness of 4μm.

The linear $1/C^2$ versus V_R characteristics in Figure 27 indicate that the impurity doping is uniform within the junction depletion region swept by the bias range of the measurement. The relationship between capacitance and reverse bias voltage, V_R, for abrupt junction is

$$(A/C)^2 = 2(V_R + V_B)(N_D + N_A)/\varepsilon q N_D N_A, \qquad (3)$$

where V_B is the built-in voltage of the junction. This voltage may be calculated, for nondegenerate doping levels, from [26]

$$V_B = (kT/q)\, \ell n(N_D N_A/n_i^2). \qquad (4)$$

An expression for n_i^2 in the GaAlAs ternary alloy is given by C.H. Henry, et al [27]

$$n_i^2 = 3.2\times10^{12} \exp(-\Delta E/kT), \qquad (5)$$

where ΔE is the difference between the bandgap of tha alloy and GaAs. From the 20AP78 solar cell spectral response the ΔE for this alloy is

0.2 eV. Assuming that $N_A = N_D = 4x10^{17} cm^{-3}$, Equation (4) yields $V_B \approx 1.5$ volts. This is reasonably close to the extrapolation of the $1/C^2$ data in Figure 27. As a result of this favorable comparison, it is concluded that no charged interface states or electric dipole layers were present at detectable levels at room temperature in these two samples.

The areas of the two devices in Figure 27 are on the order of $4x10^{-3}$ cm^2. Using this value and a relative dielectric constant of 12 for the alloy, the slope of the $1/C^2$ versus V_R data for the C20AP78 diode gives

$$N_D N_A/(N_D + N_A) = 3.8x10^{17} \text{ cm}^{-3}.$$

This value will lie between $N_{A,D}/2$ and $N_{A,D}$. This is in reasonable agreement with the initial melt doping. The inaccuracy in area measurement can introduce a fairly significant error, however.

Spectral Response of Solar Cell Structures

The spectral responses (internal collection efficiency) of two cell structures are shown normalized in Figure 28. These data are normalized because the actual active area is difficult to estimate, and no corrections were made for the reflection coefficient of the semiconductor surface. The approximate dimensions of the etched mesa were 1x1.5 mm. The data for these two cells are given in Table 4.

Table 4. Solar cell data

Sample	p-layer thickness (μm)	N-layer thickness (μm)	λ_{max}[(a)] (μm)	E_g (eV)	x_{Al}
S14AP78	1.5	6.5	0.82	1.51	0.08
S20AP78	1.0	3.0	0.76	1.63	0.19

(a) λmax is the long wavelength cutoff of the spectral response.

The apparent alloy compositions for the two cells are estimated by extrapolating the long wavelength response to zero. These compositions bracket the 14% Al alloy which is of interest for multi-junction solar cell applications. The decrease in spectral response at short wave-lengths is indicative of the detrimental effect of surface recombination.

A calculation was performed to model the spectral response of solar cell S20AP78. An electron diffusion length of 0.5 μm was assumed for the surface layer of the homojunctions. The calcuated response is given by the dashed line in Figure 28. The curve for this selection of parameters lies fairly close to the measured characteristic of device S20AP78. the amplitude of the computed spectral response at the peak is 0.386.

The measured spectral responses of both cells seem to drop more abruptly on either side of their peaks than the theoretical response. The results imply that the minority carrier diffusion lengths are certainly much less than corresponding GaAs material. For example, Hovel and Woodall chose diffusion lengths of about 2 μm in modeling their heteroface cells of GaAs[28].

The dark and illuminated current-voltage characteristics of cell structure S14AP78 are shown in Figure 29. Illumination was provided by a 600 watt tungsten halogen lamp adjusted in distance to yield an intensity of about 100 mW/cm^2 at the cell. In Figure 48, $I_{sc} \simeq 32$ mA and $V_{oc} \simeq 0.90$ volt. Based upon the approximate area of the cell mesa this gives a short circuit current density of 2.1 mA/cm^2.

III. ROCKWELL SOLID STATE ELECTRONICS LABORATORY DATA ACQUISITION SYSTEM

Background

Three separate needs have been identified for the Rockwell Solid State Electronics Laboratory (RSSEL):

1. Data acquisition and computer control of fixed station experiments. For example testing with the solar simulator.

2. Data acquisition and control for delicate or critical setups that need special considerations or for temporary test setups.

3. Data acquisition and control for the solar test facility (roof of Graham Hall)

Three subsystems are planned for the above three needs. In subsequent discussions, each system will be given a number corresponding to the data acquisition need as specified above.

All of these systems are currently under development. However, all of the equipment for the solar test facility to be located on the roof of Graham Hall have not been purchased. This report will concentrate primarily on the test setups for systems 1 and 2 as defined above.

System 1 (HP 1000 based system)

The data acquisition system for the Rockwell Solid State Electronics Laboratory (RSSEL) is designed to collect analog data and convert it to digital format to be processed by the computer. This system will help to obtain a large amount of data at a greater speed with improved accuracy. It will also assist in getting the data in

final form for papers or presentations.

Figure 31 gives the block diagram for system 1. A HP 3495 A Scanner is used as a multiplexer. Forty channels for input can be selected under program control (the number of channels can be extended up to 400). A single channel or several channels may be opened to scan a single analog signal (an output of sensor). The output of the scanner is read by the HP 3457 Digital Multimeter. The signals may be Ac, Dc or impedance. The specific function is selected under program control. The computer can be accessed using the HP 2645 Terminal. The user can communicate with the Computer HP-1000 using the interactive program (written in Fortran language). The data can be listed using the HP 9866A printer or can be plotted using the HP 9872A plotter.

Two HP 5940A HP-IB Common Carrier Interface units are required to interface instruments devices to the HP 1000. This is true because the HP-100 resides in Room 101 Graham Hall and the above-mentioned devices will reside in 128 Cherry Hall, the adjacent building.

The devices which are presently available are drawn in solid lines in Figure 31. Figure 31 also indicates some equipment (tape drive) that will be added to the system in the future. Devices to be added to the system are shown by dotted lines.

The devices which are shown in the block diagram of Figure 31 are interfaced to the HP 1000 by the HP interfacing Bus (HP-IB). Software

programs must be written to address and control each one of these devices. The last block in Figure 31 is the data file. This file is constructed through interaction with a data management program.

The data management system is depicted in Fig. 32. This system provides the user with the ability to process data off line in addition to processing in real time. A user can create a new file, or read or edit an existing file. This will provide the flexibility to recall data from previous experiments and compare (one to one or statistically) with current experiments. This is important for long term test (evaluation of solar cells) or monitoring performance of new devices fabricated and comparing the performance to previously fabricated devices or standard devices.

The user can create a new file to store all data collected and the parameters to identify the experiment. The parameters to be recorded are:

1. Date of test
2. Identification of sample or device (requires a match with an internal identification code for each sample or device to be tested.
3. Code for test description (a different code will be used for each possible test to be run). Provisions will be made to extend the code for new test setups.
4. Test parameters. A different set of parameters will be used for each test.

Once a file is created to store data, certain useful information about the file will be recorded into a directory file. The directory file contains the name of the data file, related parameters including the date the file was created, the test code number and remarks if

desired.

The directory file is a very useful document because the name, date and code of a test of interest can be obtained from the directory. This helps the user, with proper information, to recall the previous data for analysis, plotting, etc.

The user must give the file name and security code before opening the existing file for reading or editing. Once the file is opened the data can be printed, plotted, or may be processed or edited and stored in the system under a different file name.

Some of the old and unnecessary files may be purged from the system disc to save space. The use of the tape drive will also help with saving disc space. The tape drive unit will provide the main storage facility for data. Data will be recorded on tape for permanent retention and for backup to the disc files.

It should be mentioned that all the existing files are protected and can be purged only by authorized personnel.

Current Development (System 1)

1. An interactive software program has been written to give the HP 1000 Computer full control of the HP 3457A Digital Voltmeter. This program allows a number of readings at the input of DVM and prepares the data to be stored, printed or plotted.

2. An interactive software program for data management has been written. This program is responsible for all data management.

3. The file directory has been constructed which documents the file name, date data was stored, code number and remarks for all tests run under the data acquisition system.

System 2 (Desktop Computer Based System)

This system will be used for a variety of experiments that do not require high speed or large amounts of storage.

The following characteristics determine applicability:

1. Portability -- the small size and stand-alone nature of this system makes it desirable to mount it on a table with casters. It can then be used with independent, dispersed experiments that are not easily connected to centralized test equipment.

2. "Friendliness" -- This computer is particularly easy to program and operate. Thus it can be quickly adapted to fit the specific needs of an experiment that is still undergoing evaluation.

3. Dedicated -- This system is dedicated to one use and one experiment at a time. Critical or long duration experiments will suffer fewer system "crashes" that are more common on large multiprogrammed systems.

Figure 33 gives a block diagram for this system. In addition an equipment list is given below:

1 - HP-9830A Desktop Computer

   a. Basic language, extended capabilities include string variables and matrix operations.
   b. Eight thousand word read-write memory.
   c. Built-in cassette memory; cassette capacity 32,000 words.
   d. HP-9866A Printer (80 Column line printer).
   e. HP-59405A HP Interface bus interface.

2 - HP-59401A Power Supply Programmer

3 - HP-3437A System Voltmeter

4 - HP-3495A Scanner with two Duo-Decades (40 channels)

5 - HP-9872A Plotter (Four color pen plotter; plotter shared between this subsystem and subsystem 1)

Software for use in Experiment control

The flow chart for subsystem 2 as depicted in Figure 34 shows a typical process for conducting an experiment. The label on the

blocks of this flowchart refer to program modules which are described below.

The philosophy with this system is not to design a "turn-key" software system, but rather to design useful routines which can be incorporated in a main program which is written for a specific experiment. This preserves maximum flexibility while keeping program development time to a minimum. The following modules have been developed:

1. Data Gen

   This program prompts the user for voltage and time values for the experiment control stimulus. The resulting list of voltage/time pairs is stored on a tape file selected by the user.

2. Initialize

   This subprogram initializes the voltmeter, scanner and power supply.

3. FNP

   This function subroutine reads the voltage/time pair for the next stimulus. It waits until the experiment "clock" reaches the specified time, then it sets the new stimulus voltage. FNP returns value "1" to indicate when the stimulus list is exhausted otherwise it returns value "0".

4. FNS (C)

   This function subroutine sets the scanner to the channel specified in parameter (c).

5. FNV (R)

   This function subroutine causes a voltage reading to be taken on the current channel. Parameter (R) sets the voltmeter range.

6. PLOT

   This program reads the output data tape file and prints and/or plots it. One to six dependent variables are possible; each is plotted with a different color and line type. The user is prompted to input scaling and axis information for the plot.

SUMMARY

In summary, three systems for data acquisition have been planned for the Rockwell Solid State Electronics Laboratory and associated research activities. These three systems are currently under development with software being written for the first two systems. This data acquisition and management capability will significantly improve the department's ability to obtain high quality experimental results and present them in a very short period of time. Full capability for the system is anticipated by early summer, 1979.

REFERENCES

1. Hsieh, J.J., "Thickness and Surface Morphology of GaAs LPE Layers Grown by Supercooling, Step-Cooling, Equilibrium-Cooling, and Two-Phase Solution Techniques"

2. Small, M.B., Backem, K.H. and Datenski, R.M. "An Explanation for the Phenomenon of Meniscus lines on the surface of (Ga-Al) As alloys Grown by LPE", J. of Crystal Growth 39 (1977) 216-22

3. Long, S.I., "Transport Mechanisms in Liquid Phase Epitaxial Growth of Gallium Arsenide," RADC-TR-74-148, Rome Air Development Center, Griffiss Air Force Base, N.Y. 1974

4. Chandra, A. and Eastman, L., "Semiconductor Fabrication at Cornell". The Cornell Engineer Nov. 1977, Vol. 43, No. 2, pp.12

5. Bauser, E., "Development of Depressions and Voids during LPE Growth of GaAs", J. of Applied Physics, 15, 243-252 (1978)

6. Hayashi, I., Panish, M.B., Foy, P.W. and Sumski, S., Appl. Phys. Lett., 17, 109. (1970).

7. Hauser, J.R., N.C. State University, Raleigh, N.C. private communication, (February 1978).

8. Hovel, H.J., IBM J. Res. Develop. 22, pp. 111-120, (March 1978)

9. Lamorte, M.R. Hauser, J.R., Littlejohn, M.A. and Simons, M., Air Force Avionics Laboratory Technical REport AFAL-TR-77-74, Wright-Patterson AFB, Ohio,(May 1977).

10. Kagan, M.R. and Lyubashevskaya, T.L., Sov. Phys.-Semic., 1, 1091, (September 1967).

11. James, L.W., Extended Abstracts of the IEEE Electron Devices Meeting, Washington, D.C., (December 1975).

12. Milnes, A.G., Deep Impurities in Semiconductors, John Wiley, New York, (1973).

13. Sahai, R. and Harris, J.S., "Development of an (AlGaAs-GaAs) graded bandgap solar cell," Final Report, NASA CR-145161, (December 1976).

14. Moon, R.L., Varian Associates, "High Performance Gallium Arsenide Solar Cells," Quarterly Progress REport No. 2, (June 1977).

15. Fukui, T., et al., Japan J. Appl. Phys., 10, 2005, (1976).

16. Woodall, J.M. and Hovel, H.J., J. Crystal Growth, 39, 108, (1977).

17. Flat, A., Milnes, A.G. and Feucht, D. L., Solid-State Electronics, 20, 1024, (December 1977).

18. Springthorpe, A. J., King, F. D. and Becke, A., J. Electronic Mater., 4, 101, (1975).

19. Panish, M. B., J. Appl. Phys., 44, 2667, (1973).

20. van der Pauw, L. J., Philips Technical Review, 20, 220, (1958-1959).

21. Thompson, A. G. and Wooley, J. C., Can. J. Phys., 45, 255, (1967).

22. VanVechten, J. A. and Bergstresses, T. K., Phys. Rev. B, 1, (1970).

23. Hass, G., Francombe, M. and Hoffman, R., eds., Physics of Thin Films, 7, Academic Press. New York, (1973).

24. Sutherland, J.E. and Hauser, J.R., Annual Report on NASA Grant No. NSG-1116, (April 1977).

25. Wolfe, C. M. and Stillman, G. E., Appl. Phys. Lett., 27, 564, (1975).

26. Fukui, T. and Kobayashi, T., Japan J. Appl. Phys., 16, 2081, (1977).

27. Henry, C. H., Logan, R. A. and Merritt, F. R., Appl. Phys. Lett., 31, 454, (1977).

28. Hovel, H. J. and Woodall, J. M., Proceedings of the 10th Photovoltaic Specialists Conference, p. 25, Palo Alto, CA, (1973).

FIGURE CAPTIONS

Figure 1 Block diagram of the horizontal LPE growth system.

Figure 2 Assembly drawing of Graphite slider and boat.

Figure 3 Schematic Diagram of Single Layer Growth Cycle

Figure 4 Photomicrograph Epilayer (LR002-1) showing nonuniform wetting and meniscus lines.

Figure 5 Zeiss interference photomicrograph at 4x showing terracing.

Figure 6 Photomicrograph illustrating etch pits due to thermal etching.

Figure 7 Subsequent States in the Development of Depression and a Void, Schematic Cross Sections through the Crystal Solution Interface.

Figure 8 Photomicrograph of Sample #LR013-1 with the assumption of Negligible Constitutional Supercooling: (a) Surface of Epilayer 8x; (b) cleavage cross section revealing junction 16x.

Figure 9 Illustration of Dendritic Growth Projecting from the Surface of the Epilayer.

Figure 10 Microphotograph of a Cleaved Cross Section showing Dendritic Growth (16x)

Figure 11 GaAlAs solar cell efficiency as a function of percent of Al in active junction. T=500K, Conc. = 100 suns.

Figure 12 Horizontal liquid phase epitaxy system for growth of of GaAlAs layers.

Figure 13 Graphite boat and slider assembly for LPE growth of GaAlAs layers.

Figure 14 Computed liquidus-solidus data for Al-Ga-As melts.

Figure 15 Effect of Al upon As solubility in Ga.

Figure 16 Stainless steel mask pattern for etching van der Pauw samples.

Figure 17 Metal evaporation mask pattern for solar cell contact grid.

Figure 18 Photomicrograph of solar cell contact grid pattern evaporated upon LPE GaAlAs. (20AP78)

Figure 19 Spectral response measurement system.

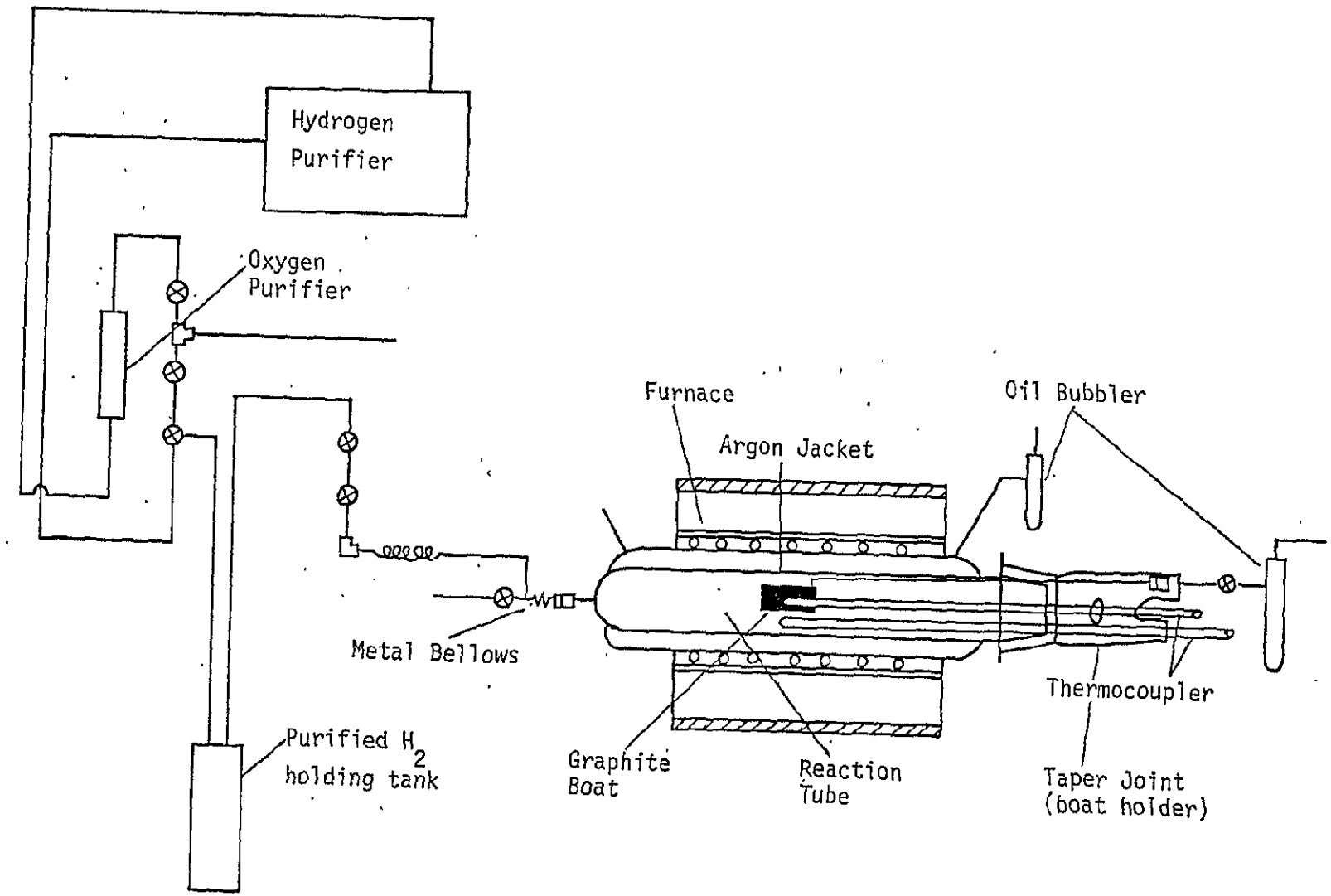
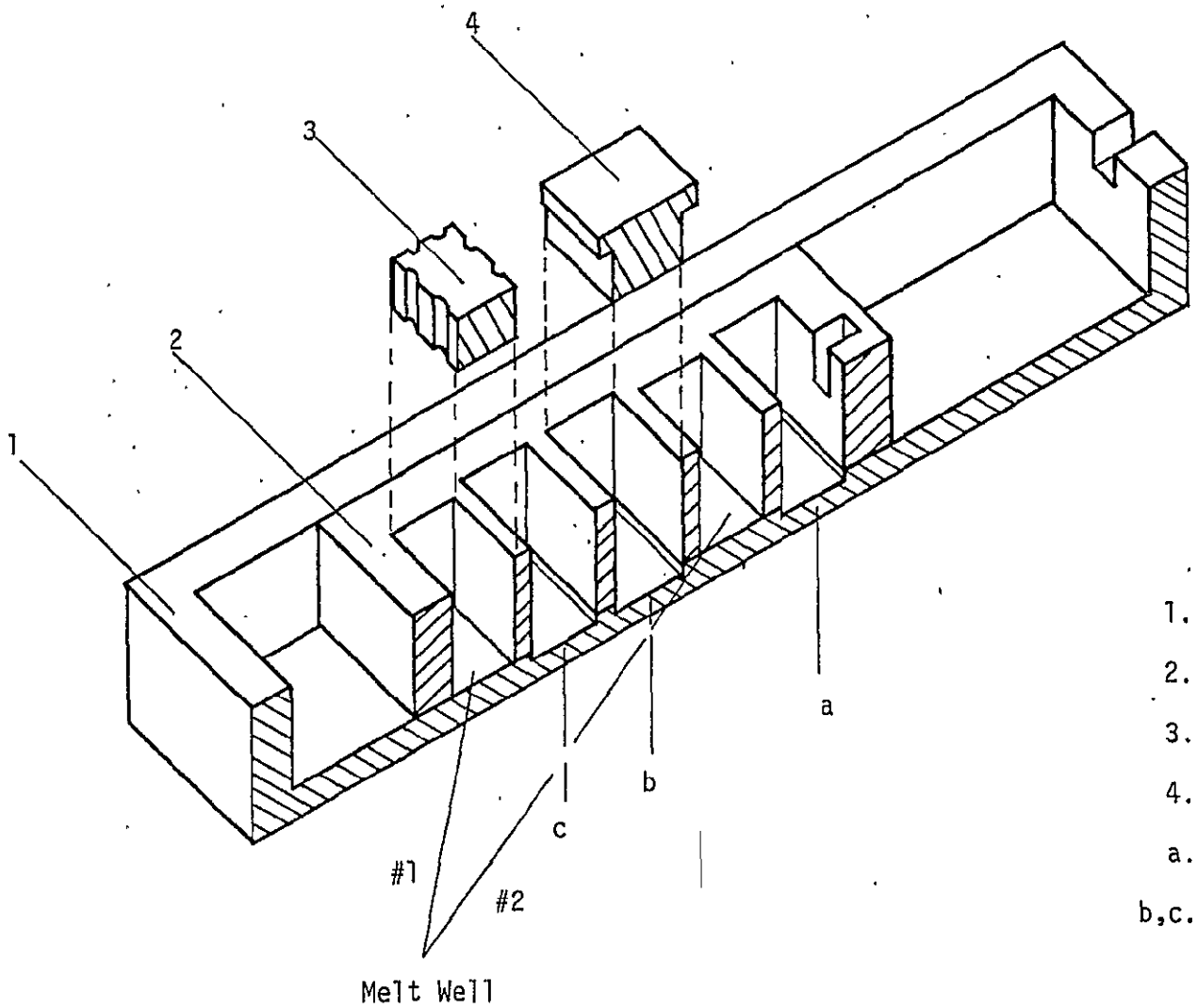

Hydrogen
Purifier
Oxygen
Purifier
Furnace
Argon Jacket
Oil Bubbler
Metal Bellows
Thermocoupler
Purified H_2
holding tank
Graphite
Boat
Reaction
Tube
Taper Joint
(boat holder)

Fig. 1



1. Boat
2. Slider
3. Melt Plunger
4. Substrate Cover

a. Substrate Recess

b,c. Source Recess

Fig. 2

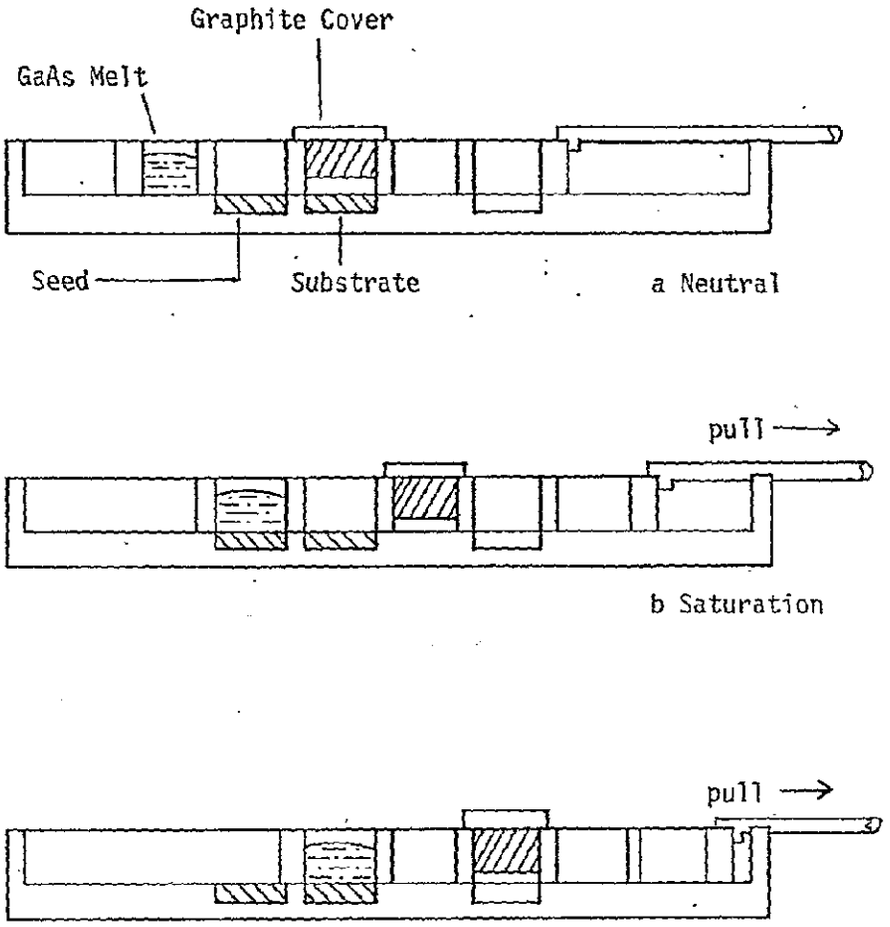

Graphite Cover
GaAs Melt
Seed
Substrate
a Neutral
pull
b Saturation
pull
c Growth of GaAs

Fig. 3

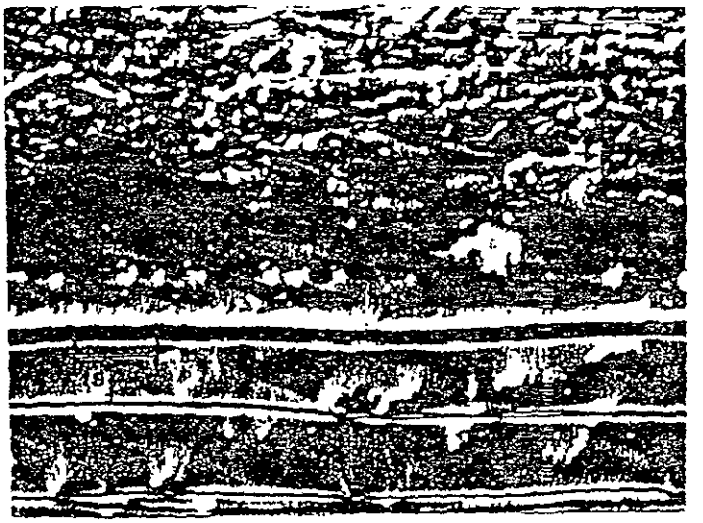


Fig. 4

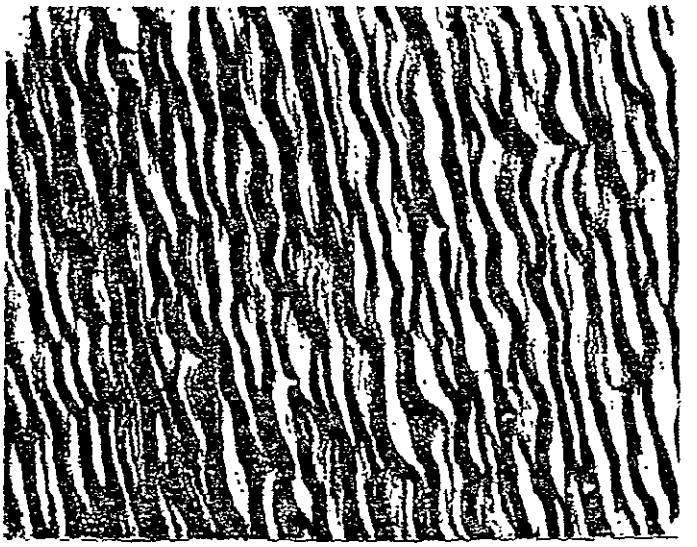
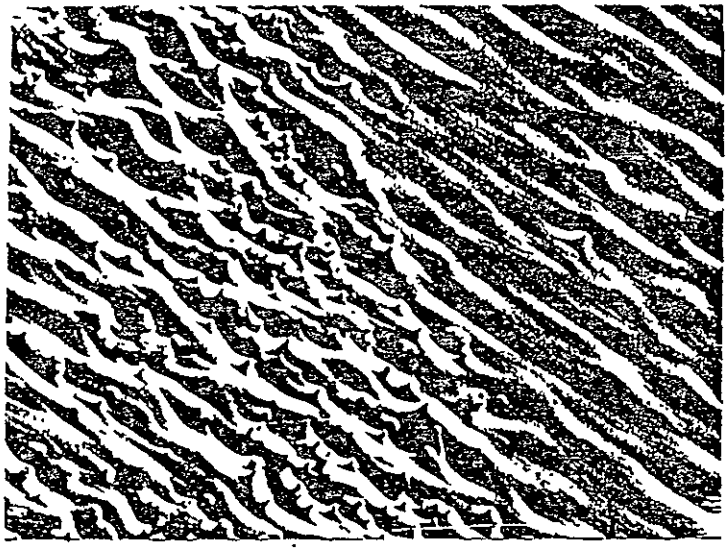
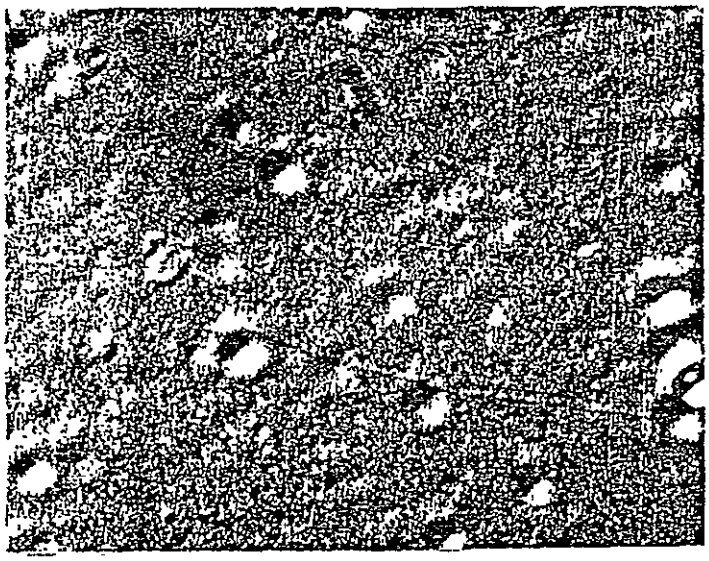


Fig. 5



(a)



(b)

Fig. 6

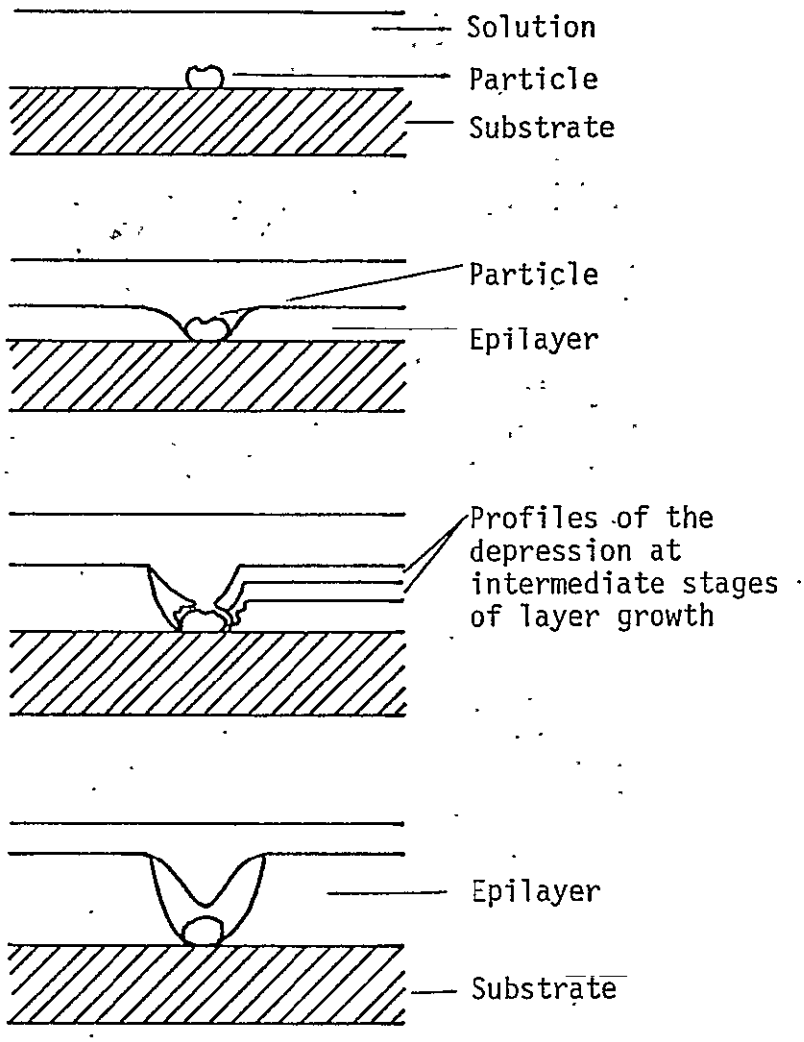
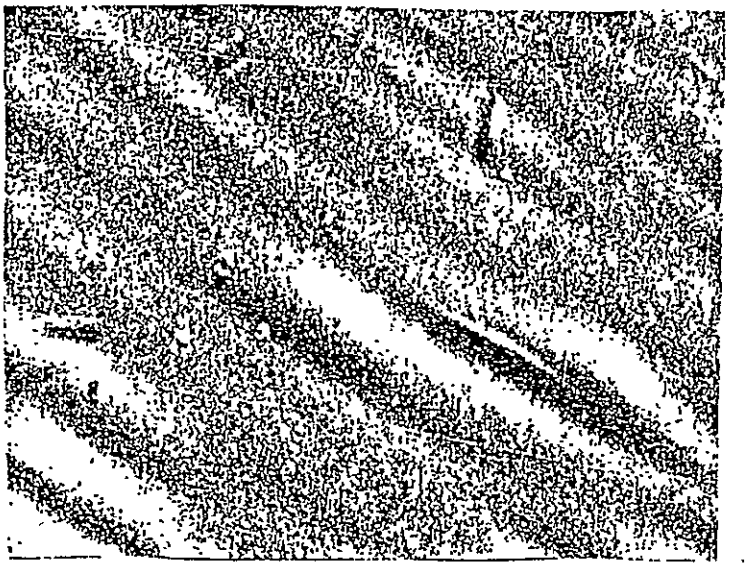
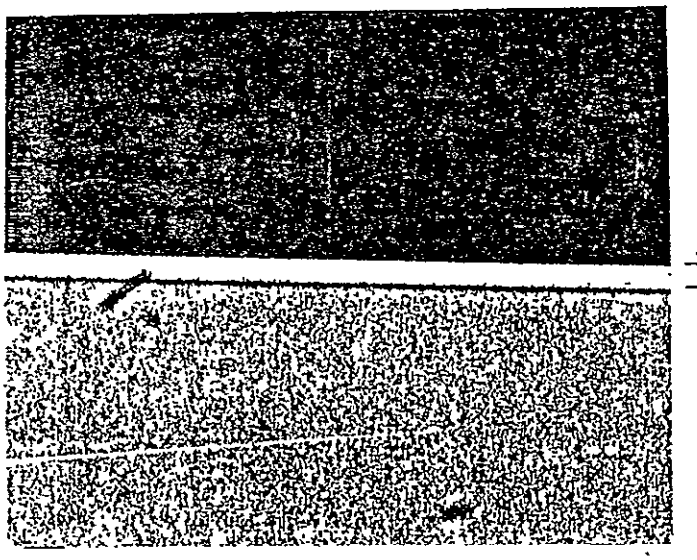

Solution
Particle
Substrate
Particle
Epilayer
Profiles of the depression at intermediate stages of layer growth
Epilayer
Substrate

Fig. 7



(a)



(b)

Fig. 8

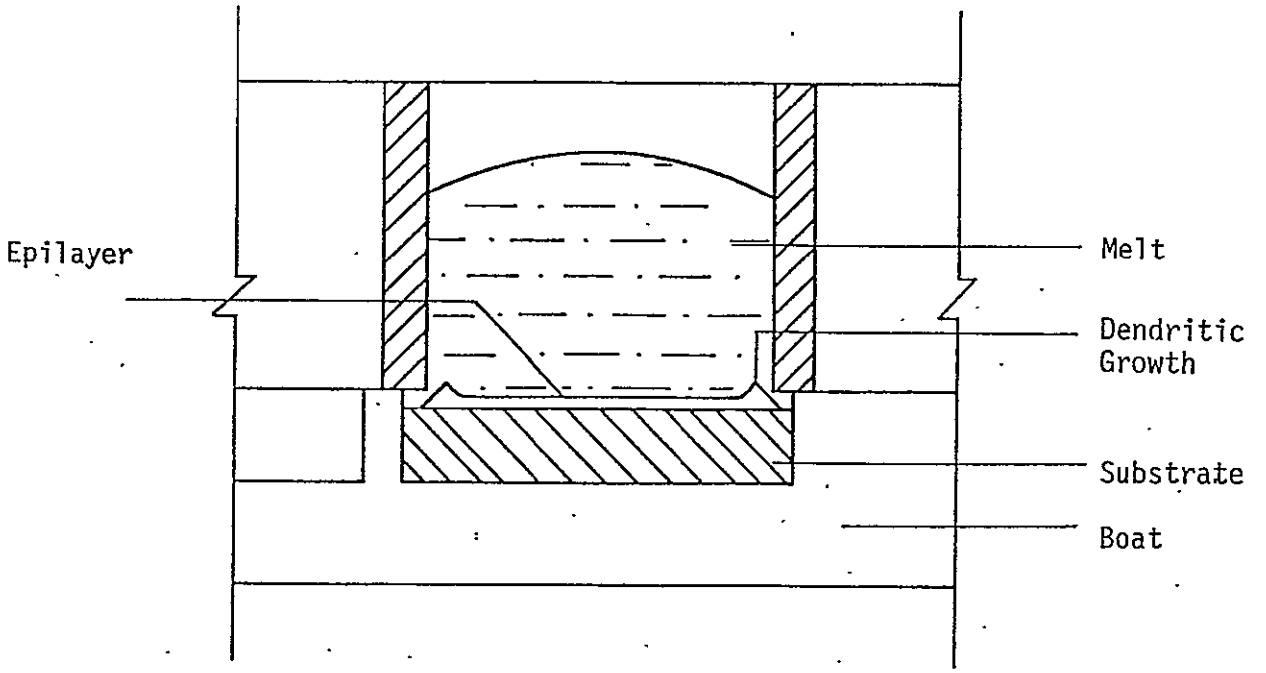


Fig. 9

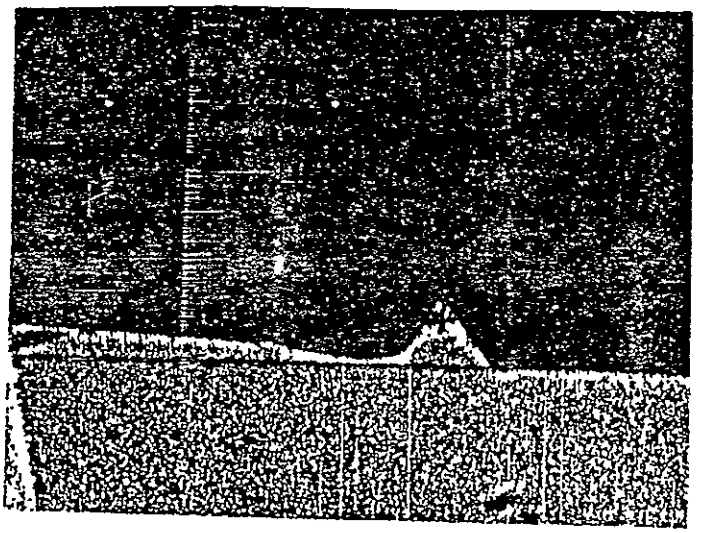
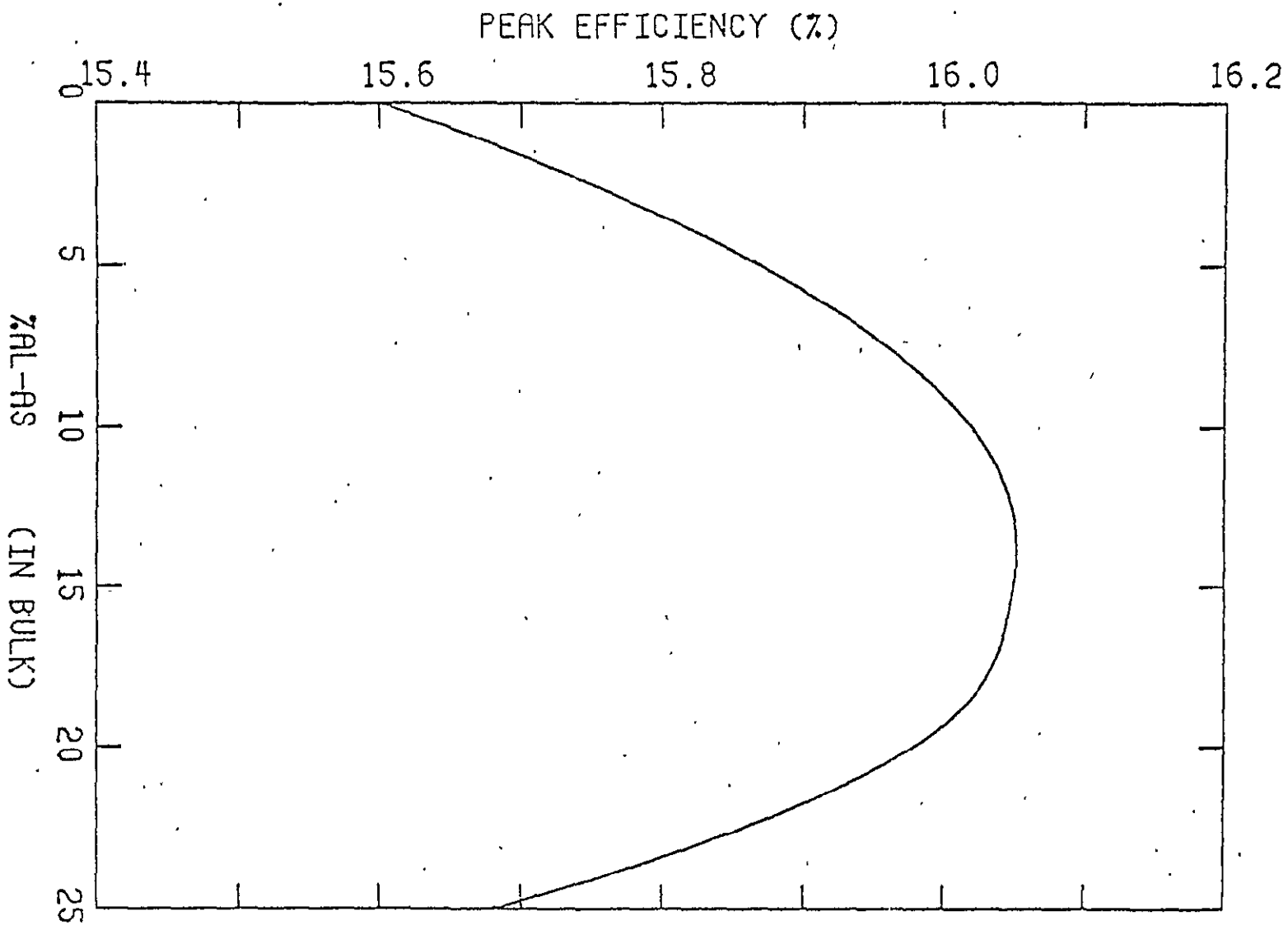


Fig. 10


PEAK EFFICIENCY (%)
15.4
15.6
15.8
16.0
16.2
0
5
10
15
20
25
%AL-AS (IN BULK)

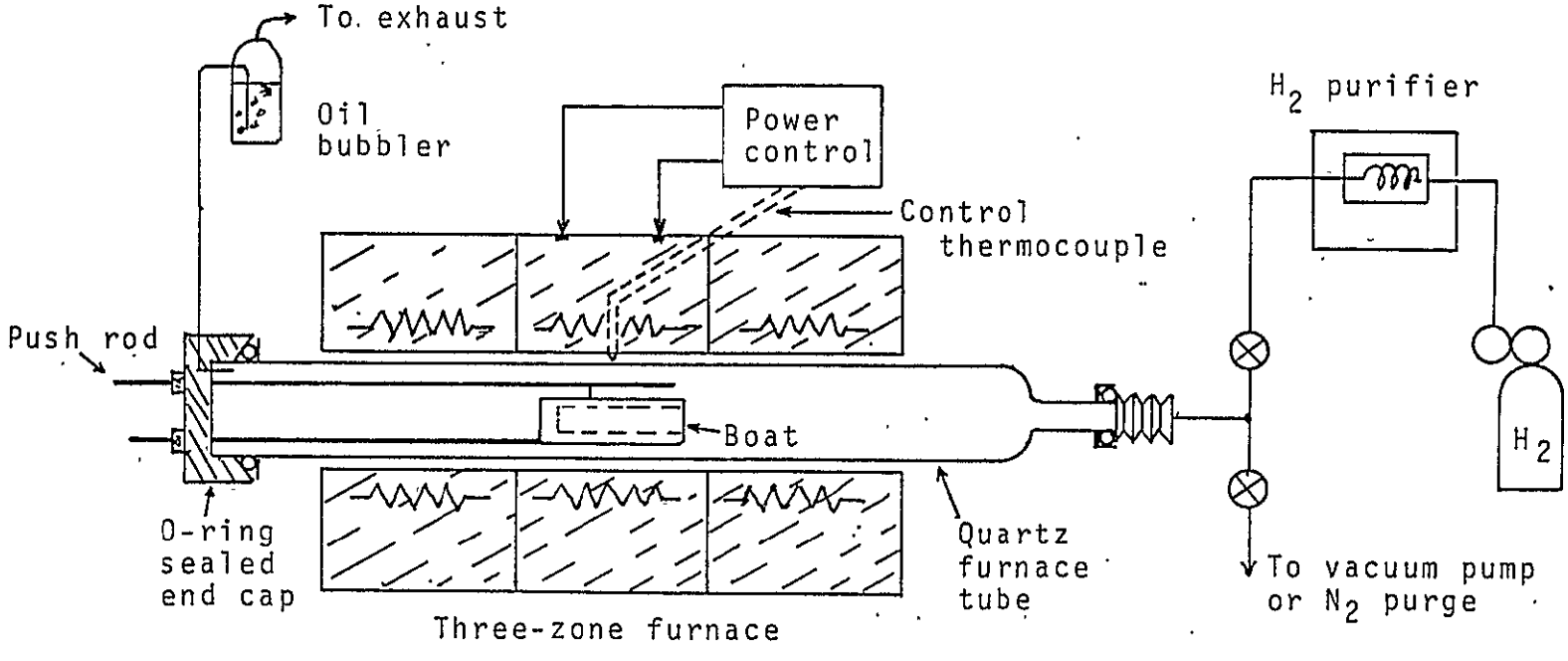

To. exhaust
Oil bubbler
Power control
Control thermocouple
H_2 purifier
Push rod
Boat
H_2
O-ring sealed end cap
Quartz furnace tube
To vacuum pump or N_2 purge
Three-zone furnace

Fig. 12

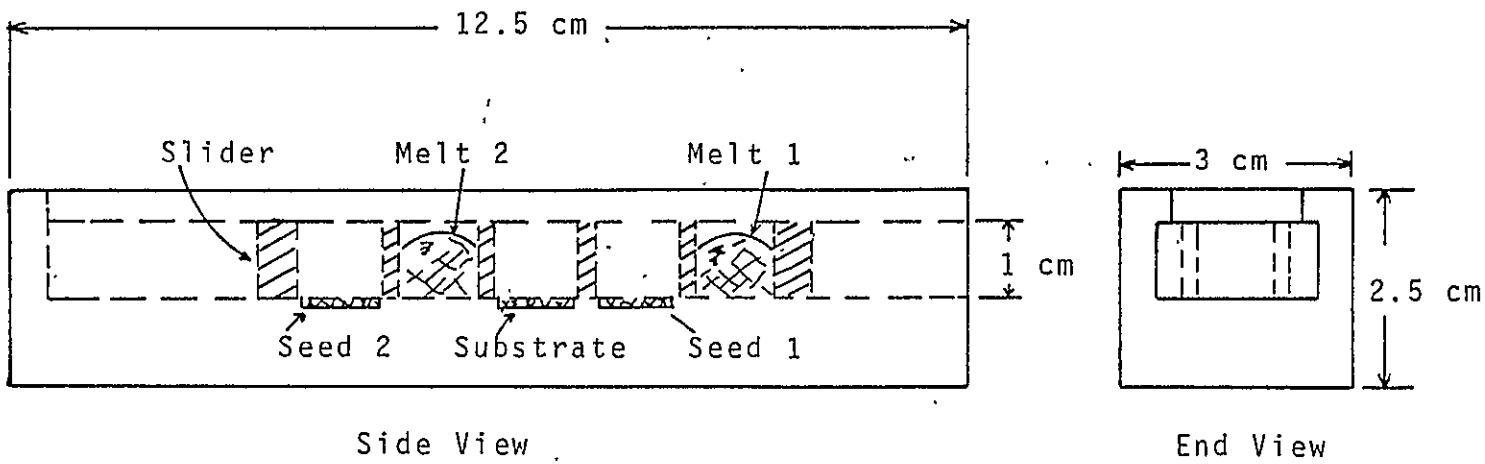

12.5 cm
Slider
Melt 2
Melt 1
1 cm
Seed 2
Substrate
Seed 1
3 cm
2.5 cm
Side View
End View

Fig. 13

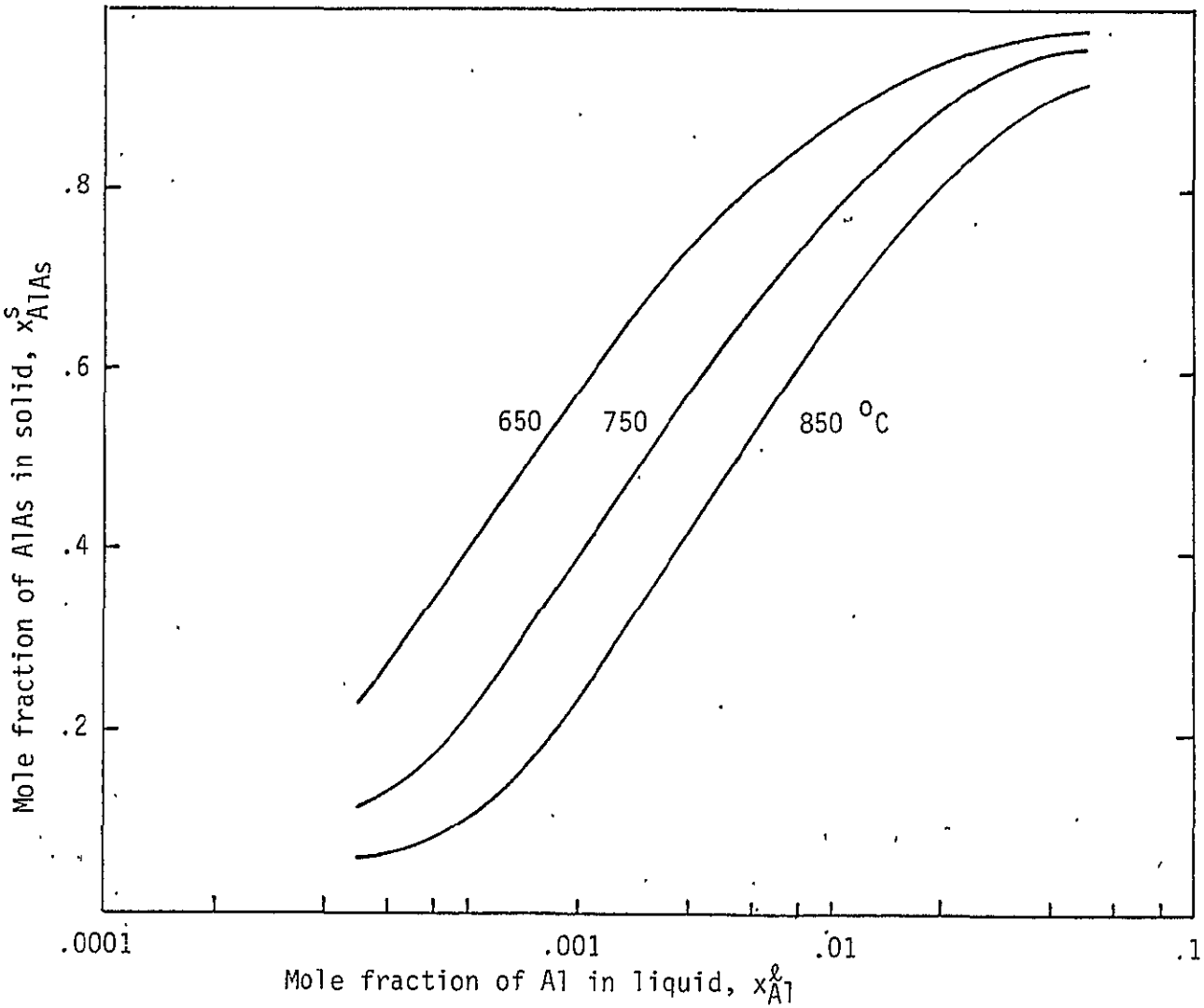

Mole fraction of AlAs in solid, x^s_{AlAs}
.8
.6
.4
.2
650
750
850 °C
.0001
.001
.01
.1
Mole fraction of Al in liquid, x^{ℓ}_{Al}

Fig. 14

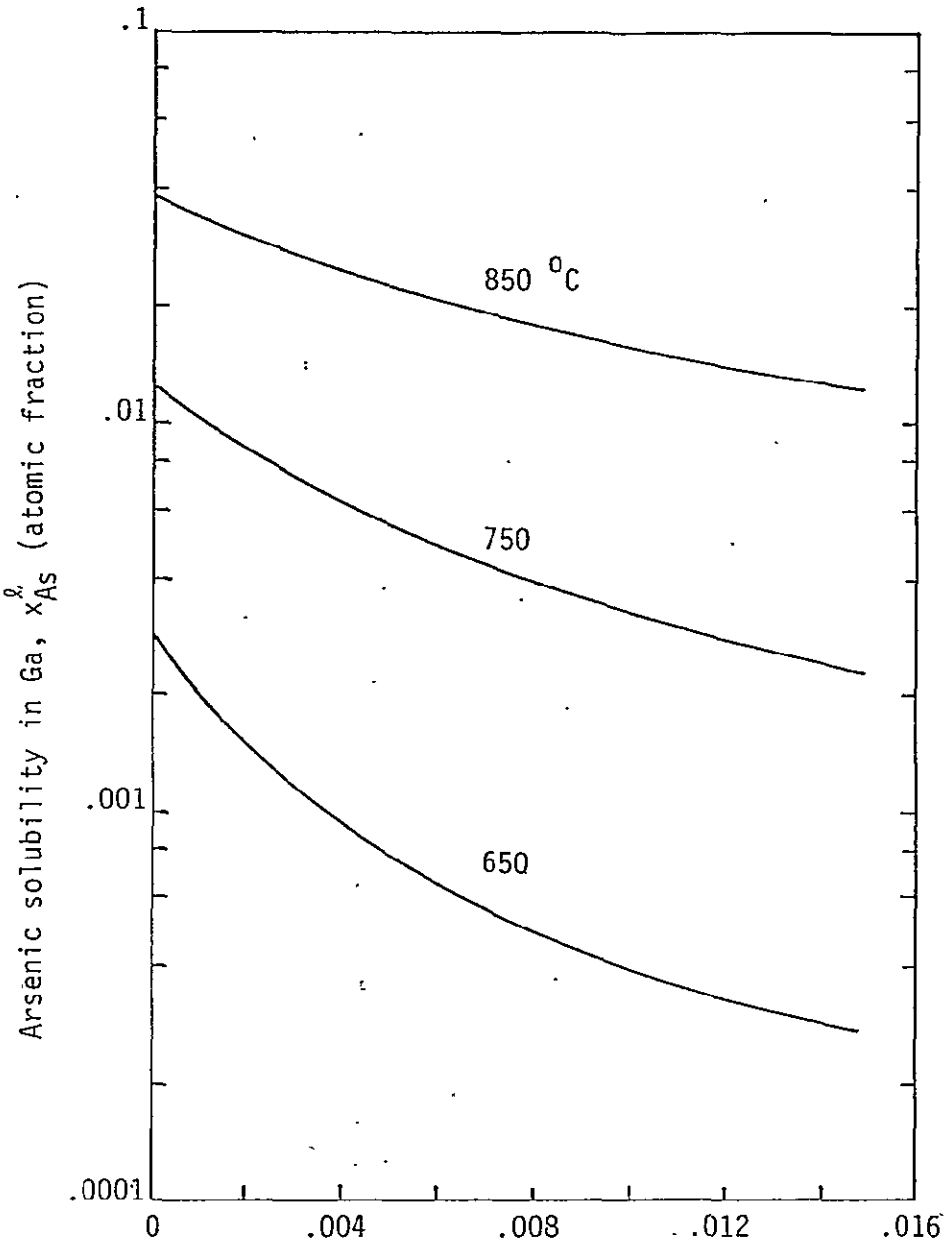

.1
.01
.001
.0001
0
.004
.008
.012
.016
850 °C
750
650
Arsenic solubility in Ga, x^{ℓ}_{As} (atomic fraction)

Fig. 15

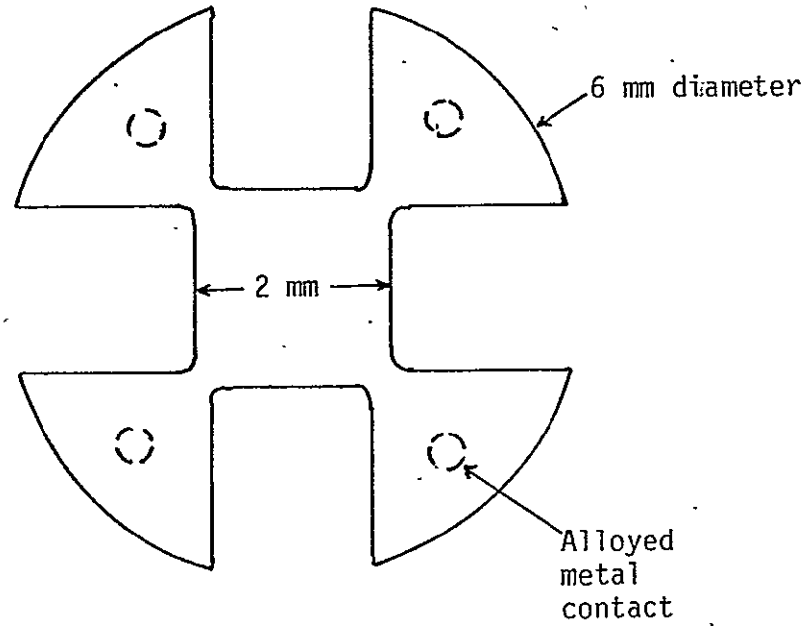


Fig. 16

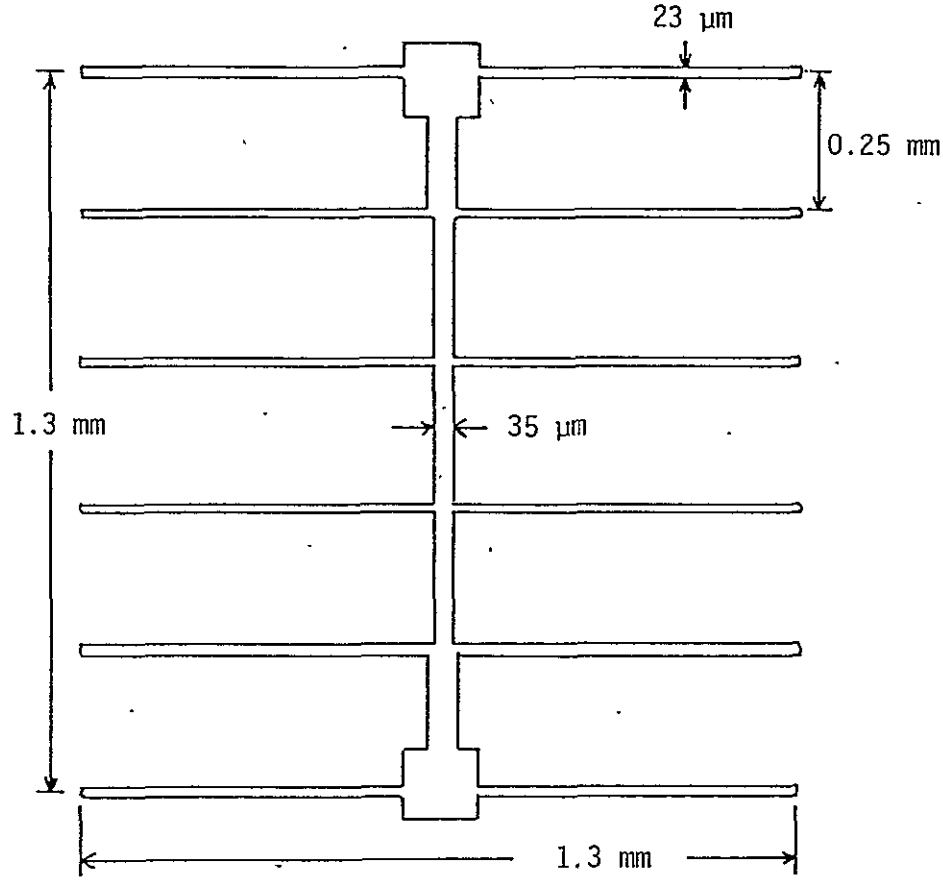


Fig. 17

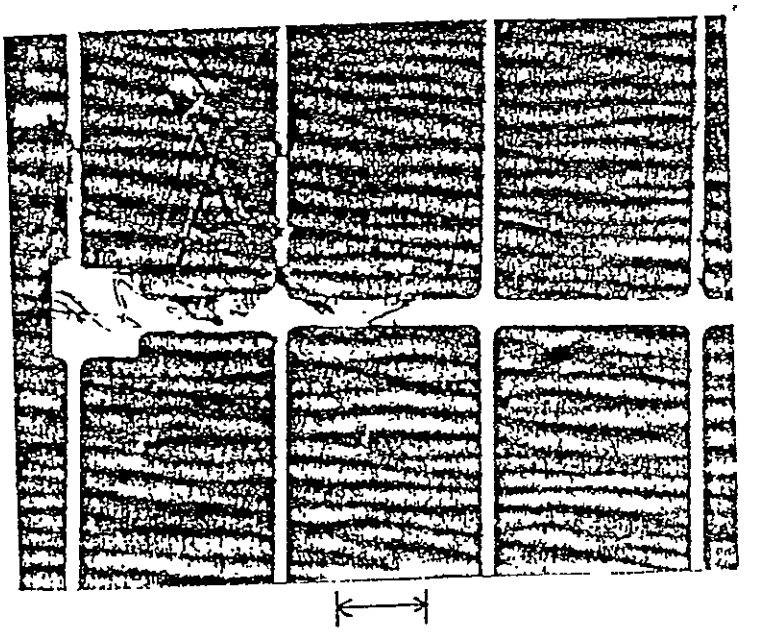


Fig. 18

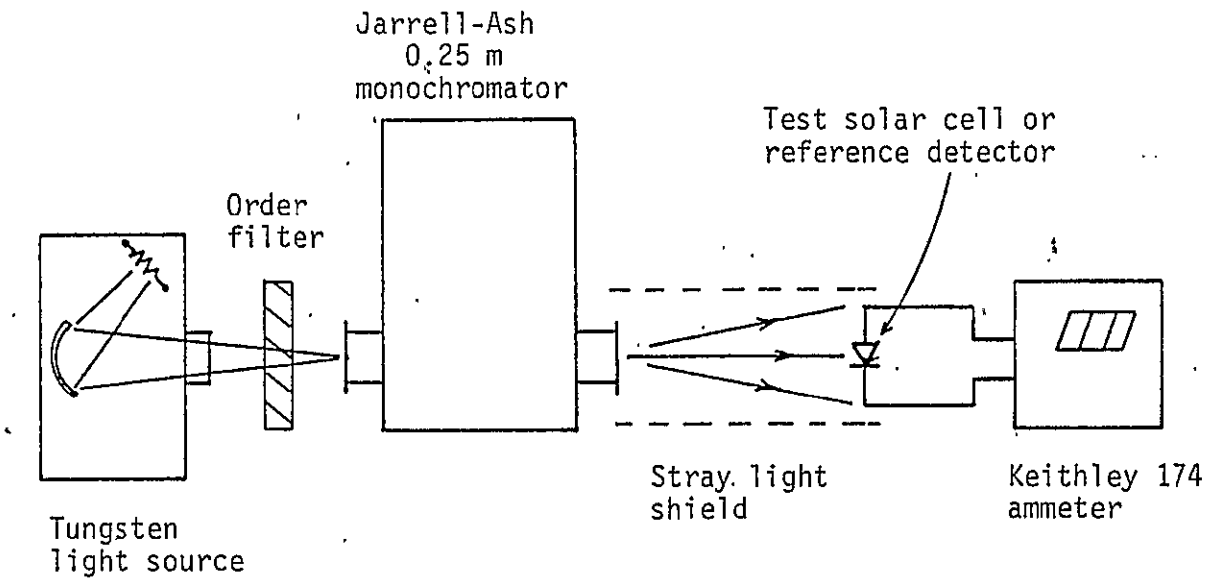
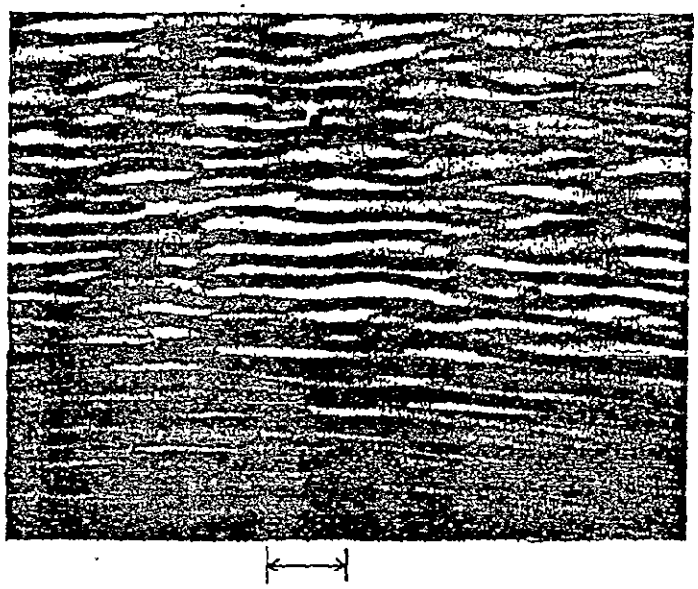

Jarrell-Ash
0.25 m
monochromator
Test solar cell or
reference detector
Order
filter
Stray light
shield
Keithley 174
ammeter
Tungsten
light source

Fig. 19



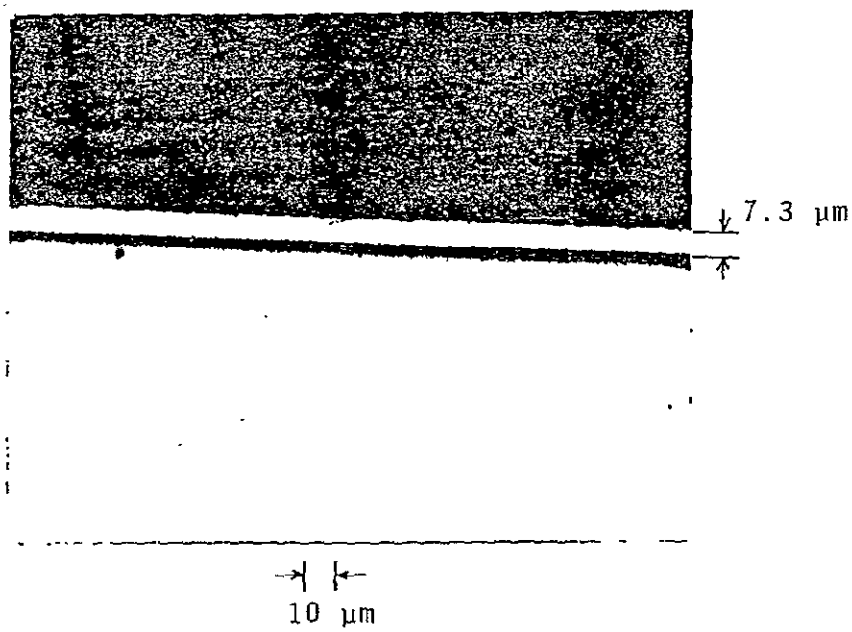


Fig. 20

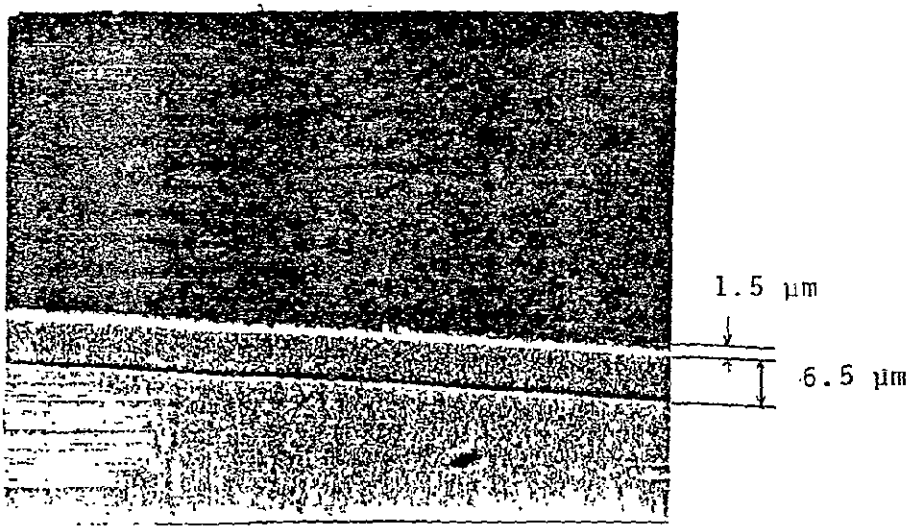


Fig. 21

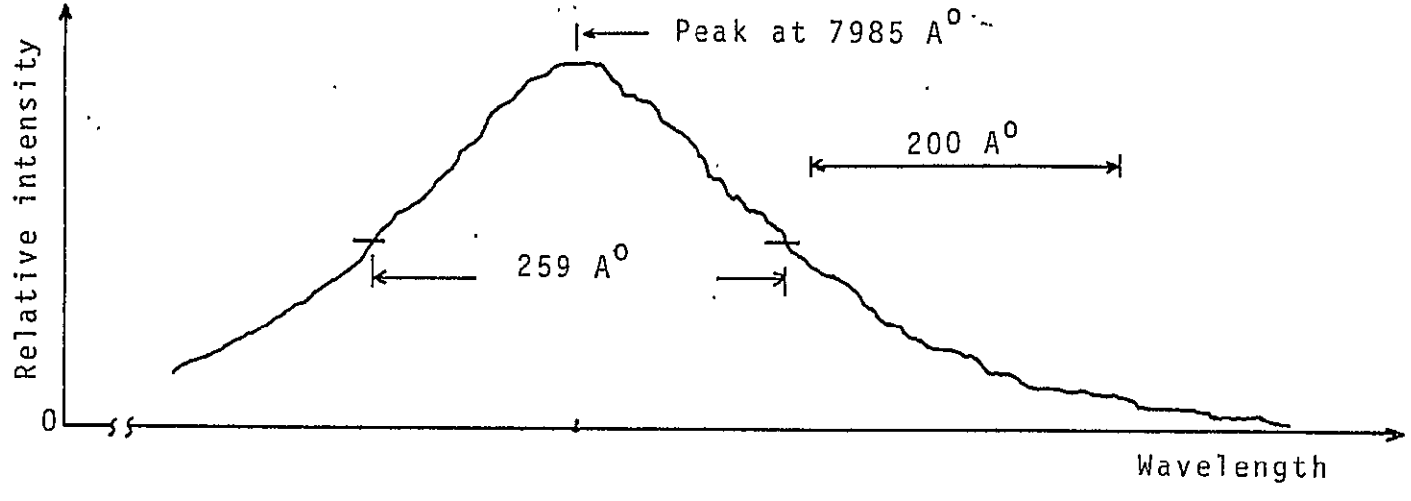


Fig. 22

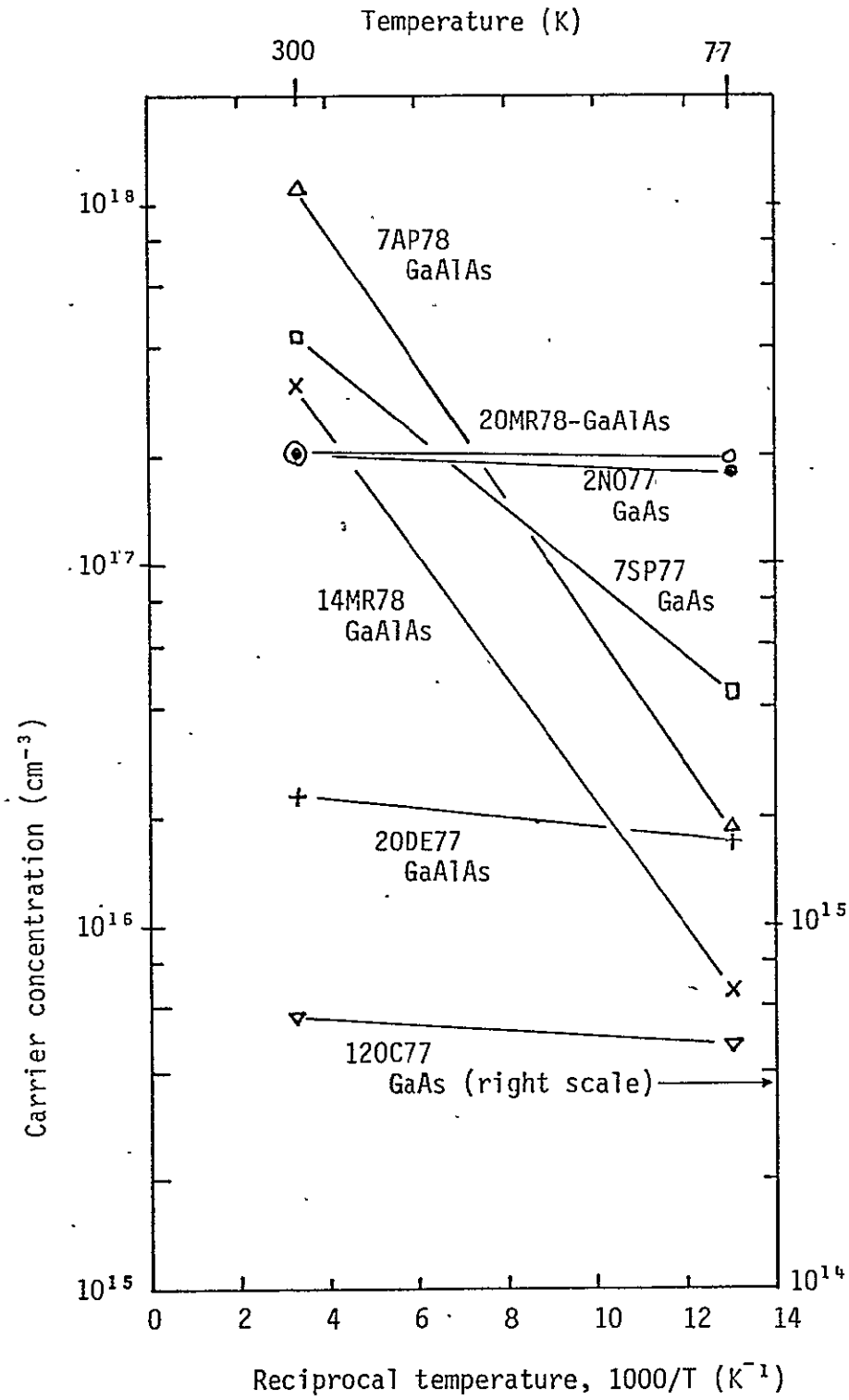

Temperature (K)
300
77
10^{18}
10^{17}
10^{16}
10^{15}
10^{15}
10^{14}
7AP78
GaAlAs
20MR78-GaAlAs
2N077
GaAs
7SP77
GaAs
14MR78
GaAlAs
20DE77
GaAlAs
120C77
GaAs (right scale)
Carrier concentration (cm^{-3})
0
2
4
6
8
10
12
14
Reciprocal temperature, 1000/T (K^{-1})

Fig. 23

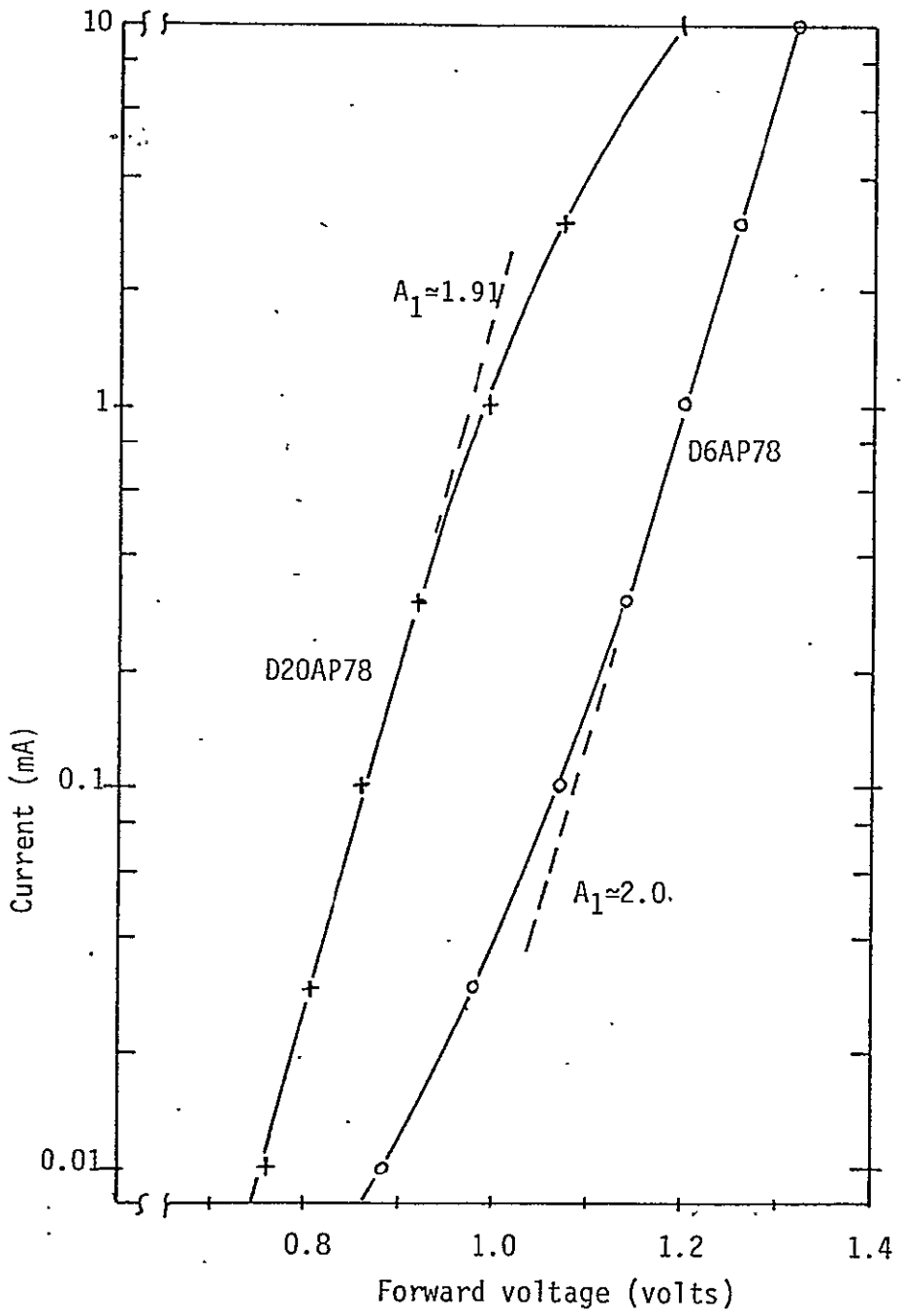

10
1
0.1
0.01
Current (mA)
0.8
1.0
1.2
1.4
Forward voltage (volts)
$A_1 \simeq 1.91$
$A_1 \simeq 2.0$
D20AP78
D6AP78

Fig. 24

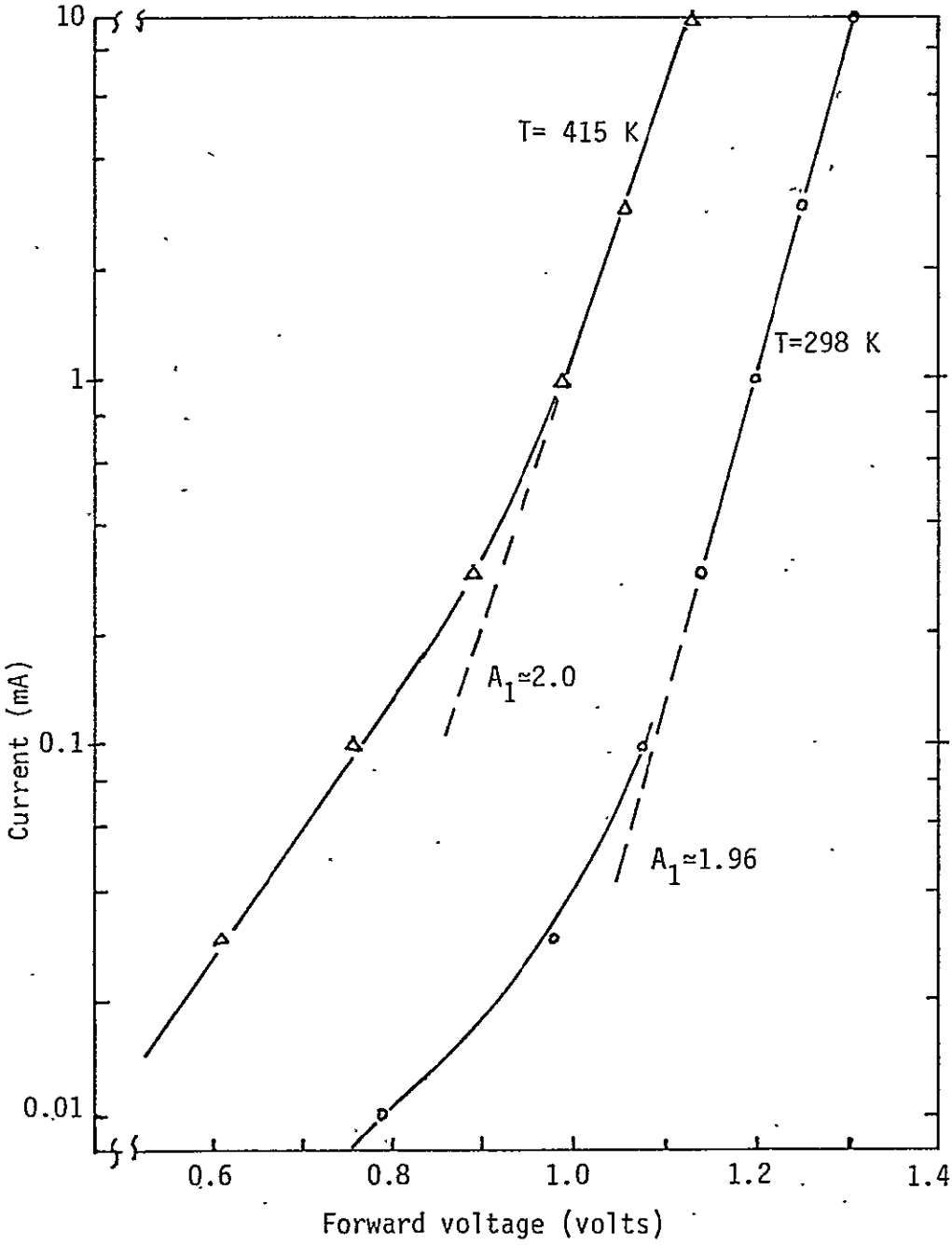

10
1
0.1
0.01
Current (mA)
T= 415 K
T=298 K
$A_1 \simeq 2.0$
$A_1 \simeq 1.96$
0.6
0.8
1.0
1.2
1.4
Forward voltage (volts)

Fig. 25

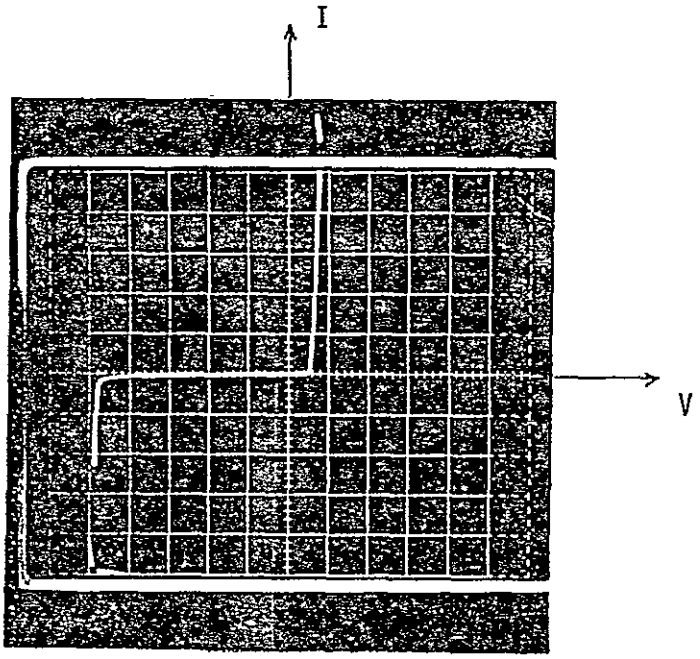


Fig. 26

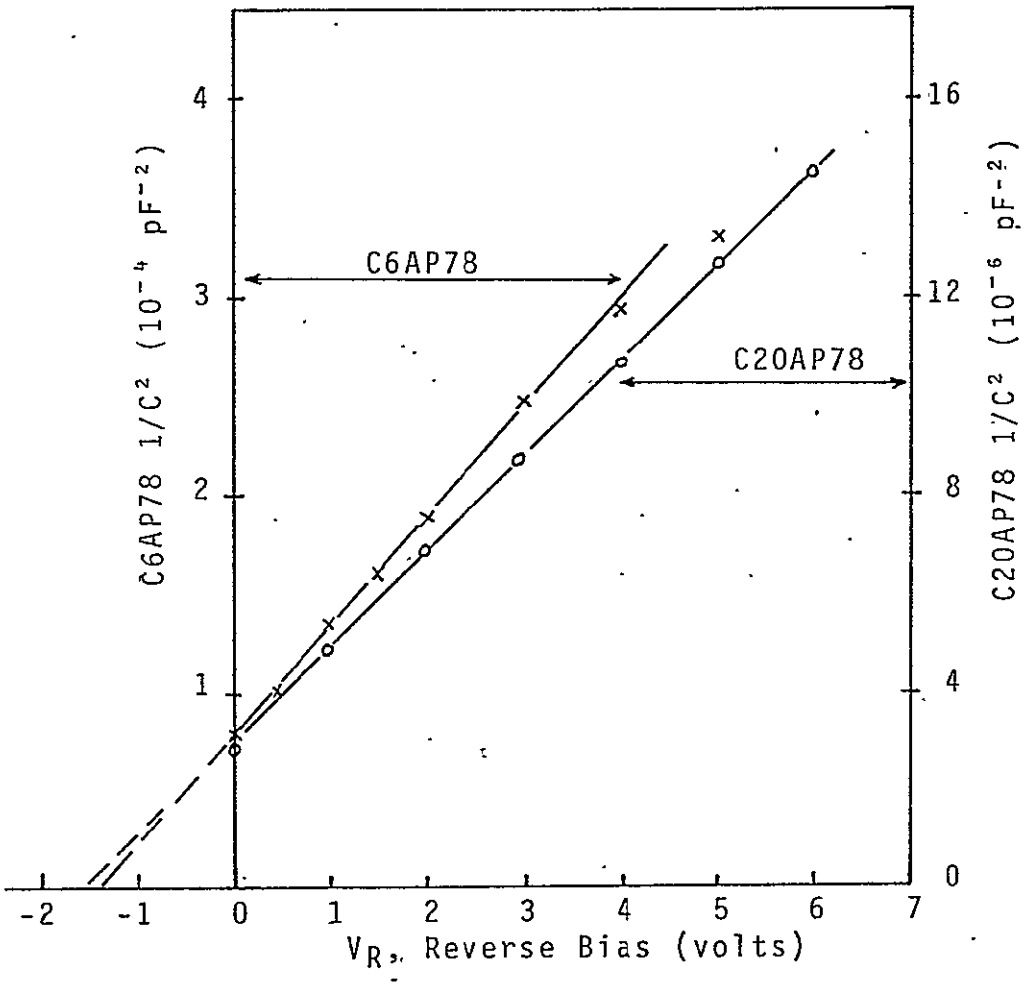

C6AP78
C20AP78
C6AP78 1/C² (10⁻⁴ pF⁻²)
C20AP78 1/C² (10⁻⁶ pF⁻²)
V_R, Reverse Bias (volts)
4
3
2
1
16
12
8
4
0
-2
-1
0
1
2
3
4
5
6
7

Fig. 27

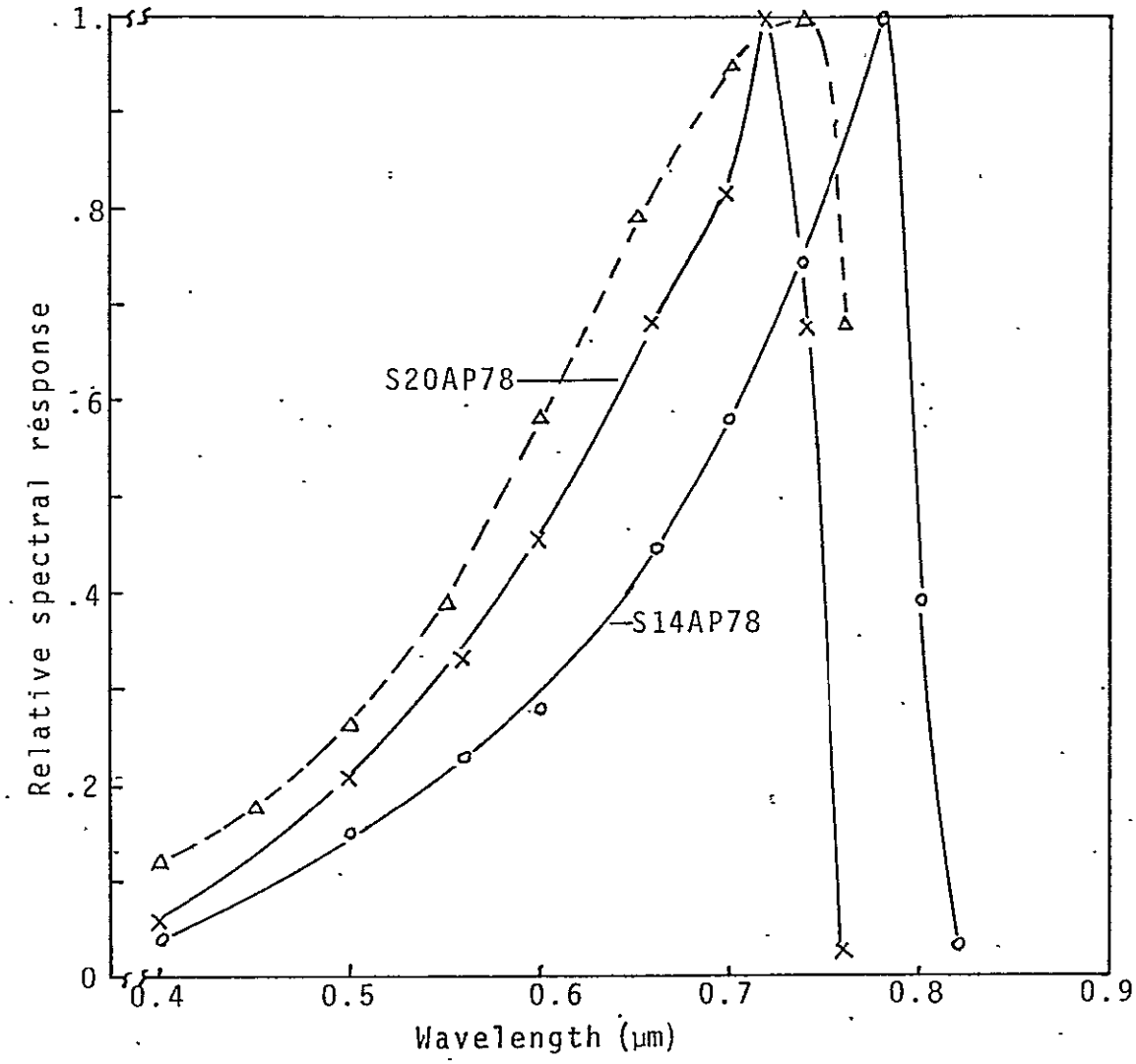

1.
.8
.6
.4
.2
0
Relative spectral response
S20AP78
S14AP78
0.4
0.5
0.6
0.7
0.8
0.9
Wavelength (μm)

Fig. 28

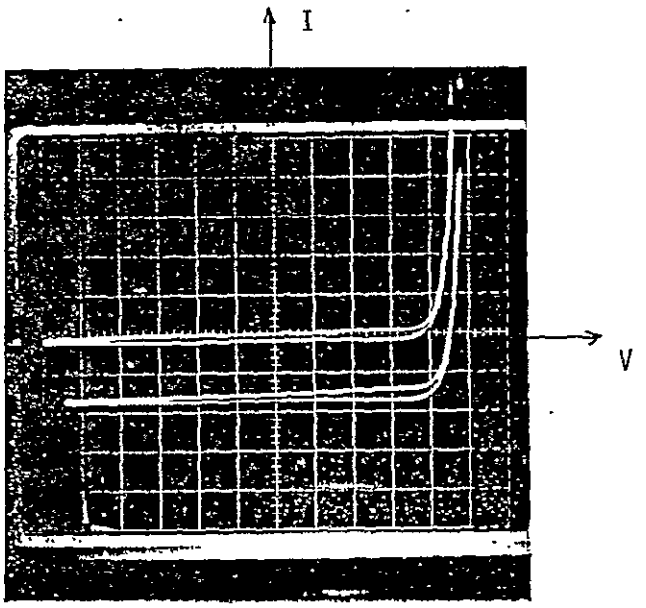
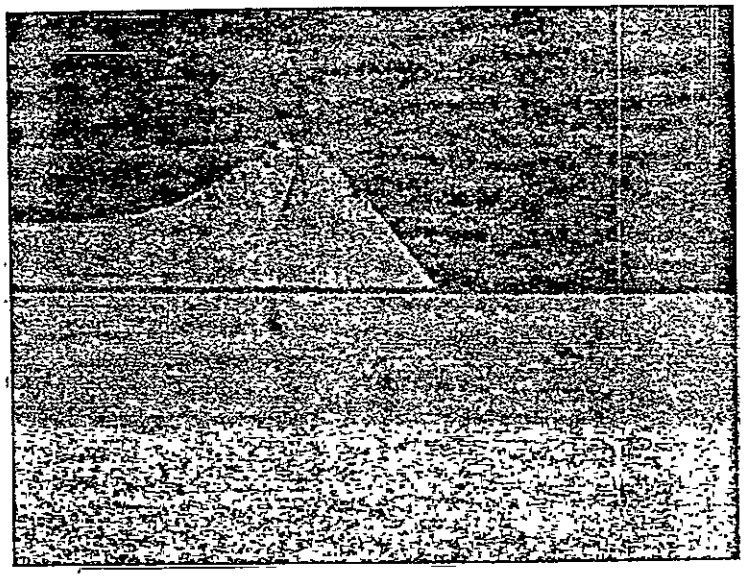
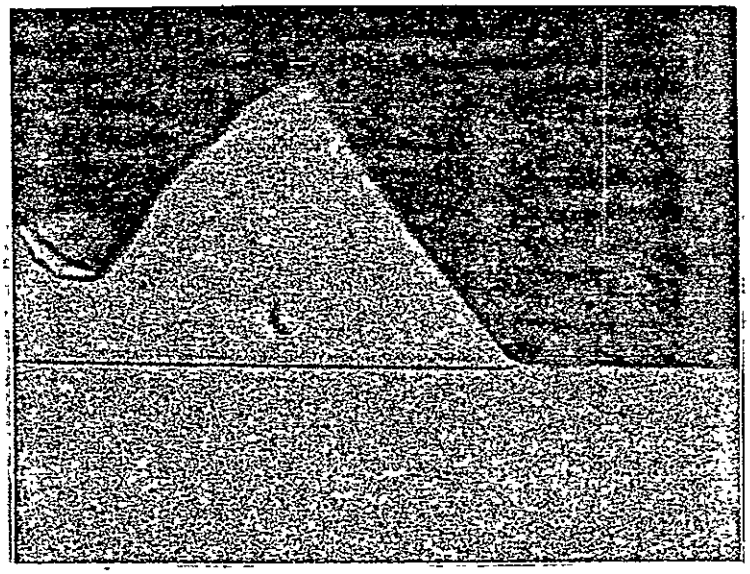


Fig. 29



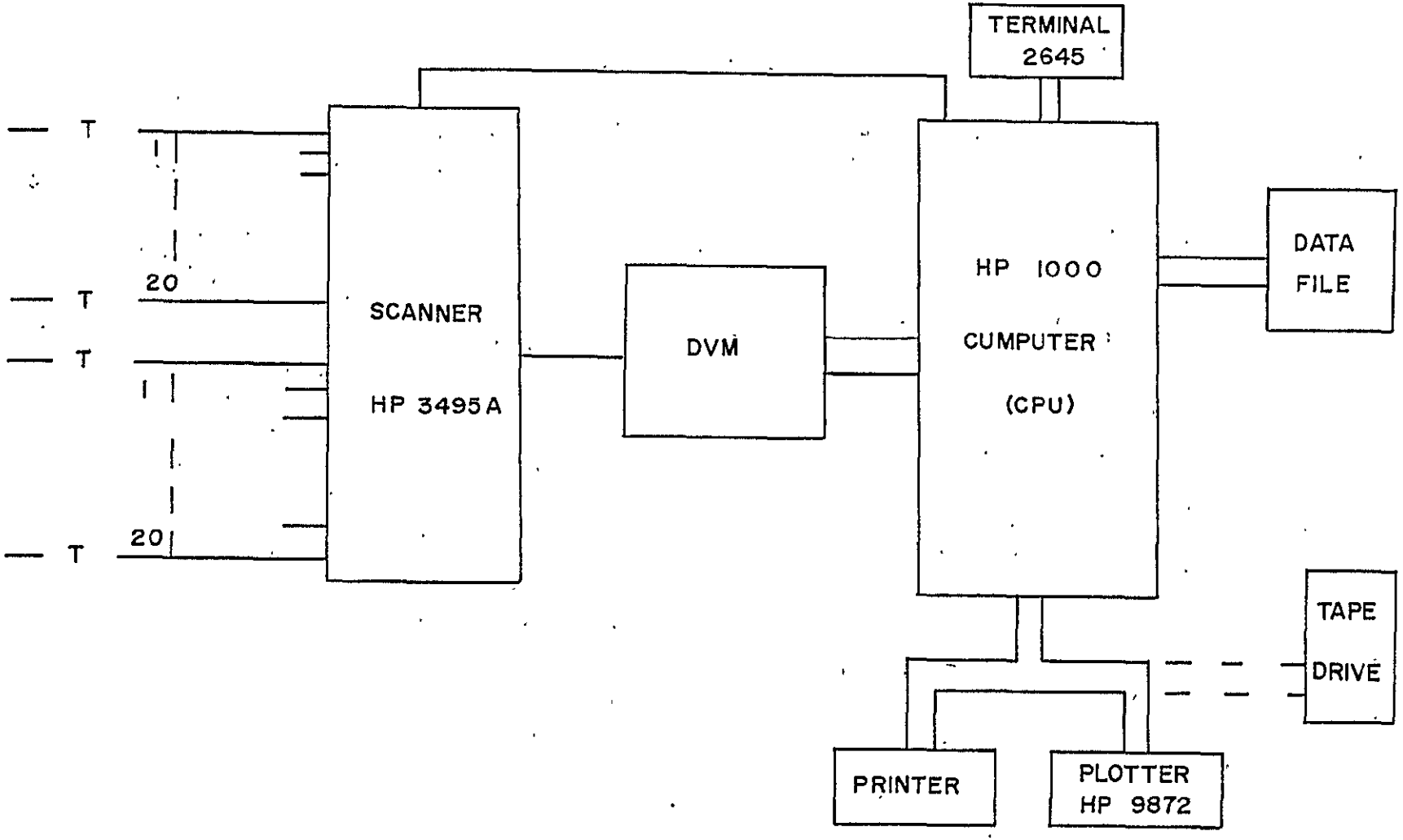
(a)

10μm



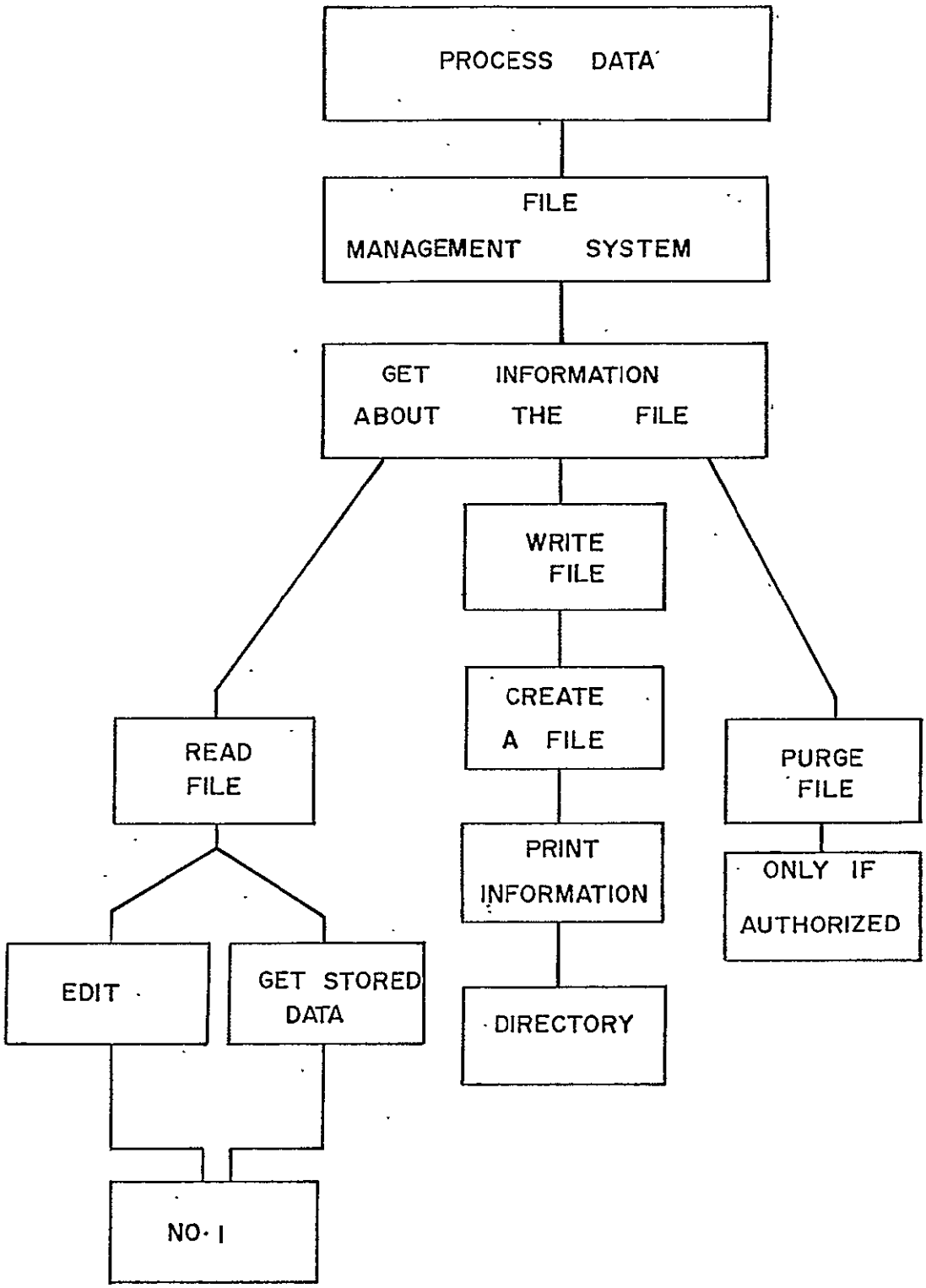
(b)

Fig. 30



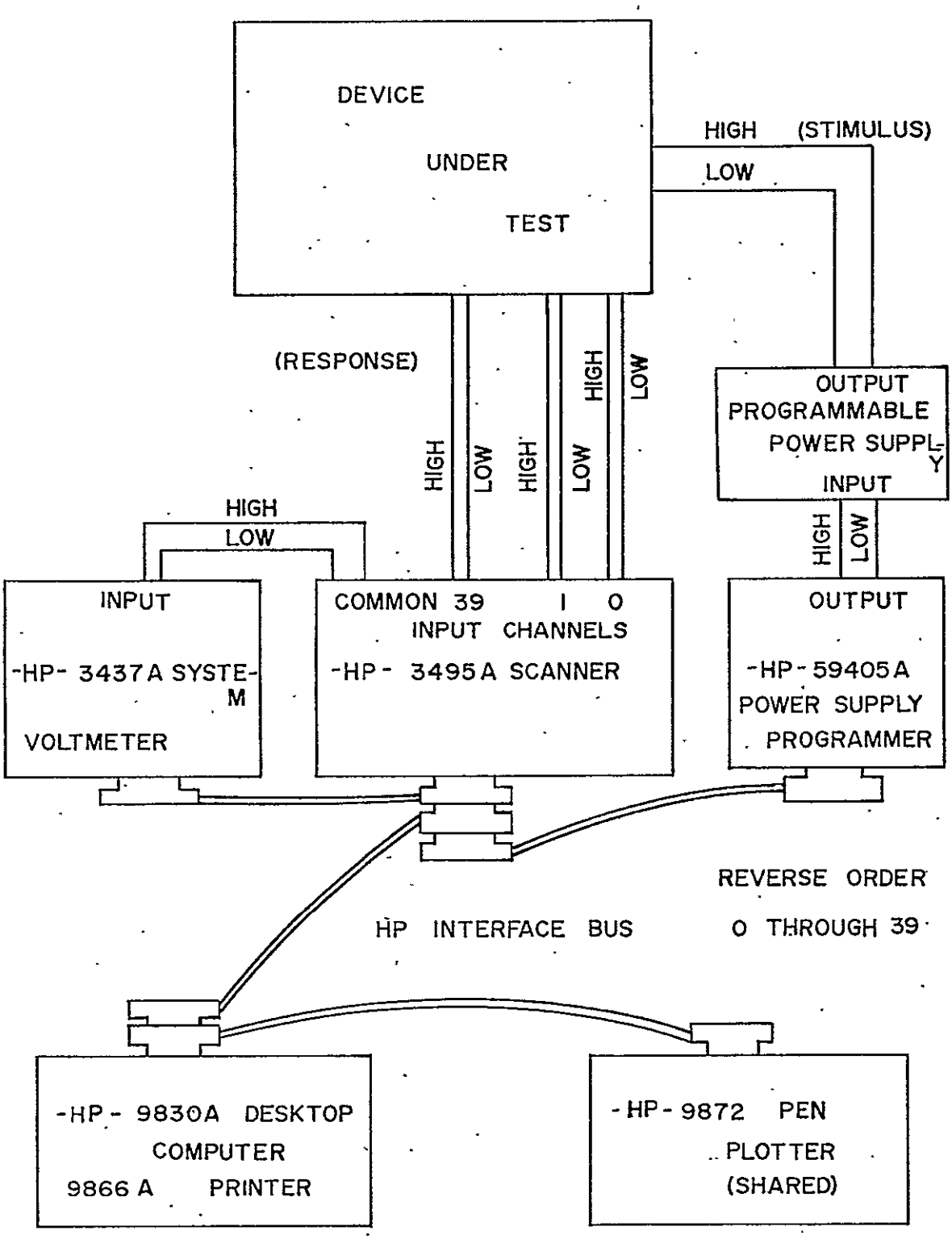
RSSEL Data Acquisition System (System 1)

Fig. 31



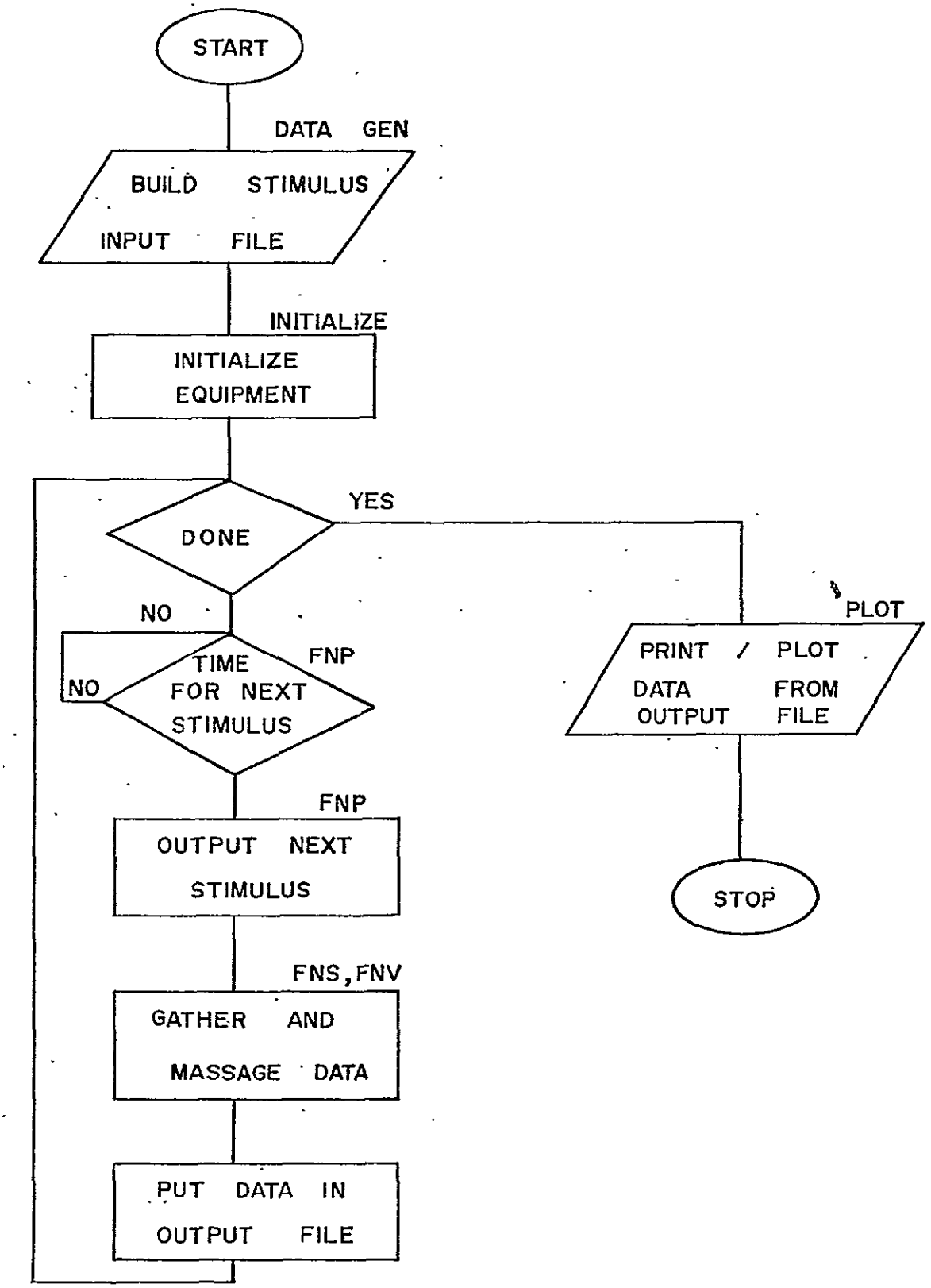
RSSEL Data Management System (System 1)

Fig. 32



Block Diagram of Desktop Computer Gased System (System 2)

Fig. 33



Flowchart of a Typical Process for Conducting on Experiment (System 2)

Fig. 34